Speck™
Dev Kit
With Optical Module
Datasheet
Jun. 2023

Outline

1. Introduction

1.1. Speck™

In the context of the traditional AI encountering bottlenecks in computational power and energy consumption, neuromorphic computing, through the inspiration from the operating mechanisms and cognitive behaviors of the biological brain, is expected to bring new exploration paths for the further development and practical application of artificial intelligence technology. By adopting bio-inspired asynchronous circuit design, the high power consumption defects brought by clock-based traditional synchronous circuit design are eliminated. As a key part of the neuromorphic intelligence system, these unique technological advantages of the neuromorphic chip greatly enhance the utilization rate of hardware resources and the operational efficiency of pulse neural networks.

Speck™ is the world's first "sensor-compute integrated" neuromorphic intelligent dynamic vision SoC, integrating an asynchronous neuromorphic dynamic vision processor (DYNAP™CNN) and a Dynamic Vision Sensor (DVS), also known as an Event Camera, Dynamic Event-based Sensor (DES), or Event-based Vision Sensor (EVS). It features a large-scale spiking convolutional neural network (sCNN) chip architecture based on an asynchronous logic paradigm, configurable with up to 320,000 spiking neurons, and internally integrates the state-of-the-art event-based, 128x128 resolution dynamic vision sensor (DVS) for real-time and efficient dynamic vision input.

Speck™ paves the way for always-on IoT devices and applications such as edge computing and human-machine interaction, behavior recognition, gesture recognition, facial detection, human tracking, and surveillance, with ultra-low power consumption and ultra-low latency.

1.2. Speck™ dev kit (with optical module)

Speck™ dev kit (with optical module) is powered by the SynSense Speck™ chip optical module (Currently, there are two specifications equipped with 3.62mm/1.98mm lens.), which brings the flexibility of convolutional dynamic vision processing to milliwatt energy budgets. It provides the capabilities for real-time presence detection, real-time gesture recognition, and real-time object classification.

Development of up to nine-layer spiking convolutional networks to process the output of

the internal dynamic-vision sensor is made easy with our open-source Python library Sinabs and SynSense device toolchain Samna.

Figure 1 . Speck™ dev kit (with optical module)

2. Features

2.1. Speck™ SoC chip

2.1.1 Key features

- 1 Built-in DVS layer
- 9 DYNAP™CNN layer
- 1 Readout layer
- SPI slave/master instarface
- Sum pooling {1:1, 1:2, 1:4}
- Fanout of 2
- Ultra-low average working power consumption

2.1.2 DVS layer

- 128x128 array
- Noise filtering

- DVS polarity adjustment
- ROI selection
- Mirroring in both X/Y
- Rotate in 90-degree steps
- Dynamic range not less than 80 dB (20-200k lux)

Note: When used between 20lux to 50lux, there is a slight decrease in the sensitivity of the optical sensor array, and there may be a slight increase in the delay of the algorithm model. There is a possibility of occasional missed or erroneous judgments (with a probability of less than 5%, see Chapter 8.1 in the appendix).

2.1.3 DYNAP™-CNN computing layers

- Up to 9 CNN layers
- Max input dimension 128*128
- Max feature output size 64*64
- Max feature number 1024
- Weight resolution 8 bits
- Neuron state resolution 16 bits
- Max kernel size 16*16
- Stride {1,2,4,8} independent in X/Y
- Padding [0..7] independent in X/Y
- Pooling 1: 1, 1:2, 1:4
- Fanout of 2
- Leak operation on each layer
- Spike decimator on each layer
- Spike congestion balancer on each layer
- Parallel computing on layer 0 and layer 1, enabling larger throughput, can be used as input layers

2.1.4 Readout layer

- 15 classes and 1 idle class
- Selectable moving average between 1, 16 and 32 time steps.
- 4 readout modes: inactive/threshold/max spiking class/specific class.
- 4 readout pins and 1 interrupt pin

2.2. Dev kit

- Speck™ optical module equipped with 3.62mm/1.98mm lens, for more details,

please refere to Chapter 3.1

- 1x USB 3.0 Micro-B port
- On board power monitor over five power traces: VDD_IO, VDD_RAM,VDD_LOGIC, VDD_PIXEL_DIGITAL, VDD_PIXEL_ANALOG of Speck™ SoC
- Speck™ readout pin monitoring through Samna

3. Mechanical specification

3.1. 3.62mm optical module specification

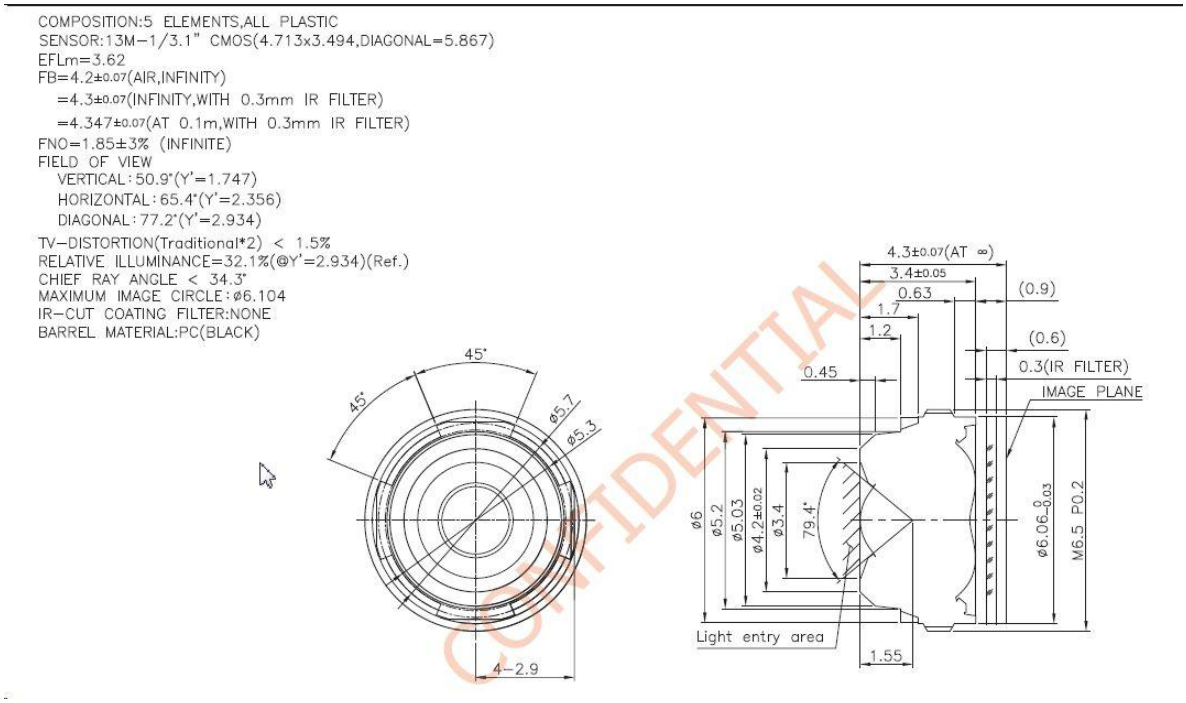


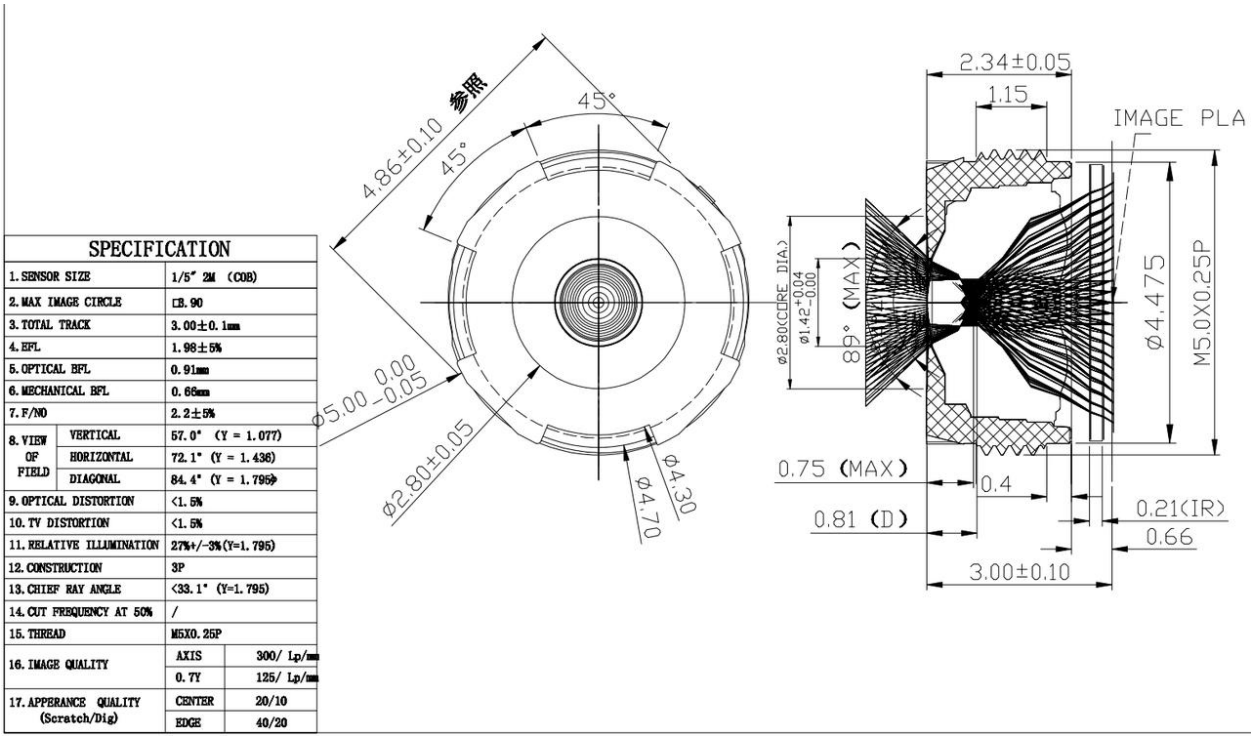
Figure 2 . Specification of the 3.62mm lens

The quick calculation formula for the field of view angle of a DVS sensor under different focal length lenses is:

HFOV = 2 * ARCTAN(H / (2 * EFL)), VFOV = 2 * ARCTAN(V / (2 * EFL))

For example, the H-FOV of SYNS91105M (3.62mm) is 38.95°, and the V-FOV is also 38.95°. (Here, H = V = 2.56mm, EFL is the focal length of the lens (3.62mm), H-FOV is the horizontal field of view angle, and V-FOV is the vertical field of view angle).

3.2. 1.98mm optical module specification



SPECIFICATION			
1. SENSOR SIZE		1/5" 2M (COB)	
2. MAX IMAGE CIRCLE		□3.90	
3. TOTAL TRACK		3.00±0.1mm	
4. EFL		1.98±5%	
5. OPTICAL BFL		0.91mm	
6. MECHANICAL BFL		0.66mm	
7. F/NO		2.2±5%	
8. VIEW OF FIELD	VERTICAL	57.0° (Y = 1.077)	
	HORIZONTAL	72.1° (Y = 1.436)	
	DIAGONAL	84.4° (Y = 1.795)	
9. OPTICAL DISTORTION		<1.5%	
10. TV DISTORTION		<1.5%	
11. RELATIVE ILLUMINATION		27%+/-3%(Y=1.795)	
12. CONSTRUCTION		3P	
13. CHIEF RAY ANGLE		<33.1° (Y=1.795)	
14. CUT FREQUENCY AT 50%		/	
15. THREAD		M5X0.25P	
16. IMAGE QUALITY	AXIS	300/ Lp/mm	
	0.7Y	125/ Lp/mm	
17. APPERANCE QUALITY (Scratch/Dig)	CENTER	20/10	
	EDGE	40/20	

Figure 3 . Specification of the 1.98mm lens

According to the formula:

HFOV = 2 * ARCTAN(H / (2 * EFL)), VFOV = 2 * ARCTAN(V / (2 * EFL)),

The H-FOV=65.8°，V-FOV=65.8°（where H = V = 2.56mm）for 1.98mm lens.

3.3. Speck™ dev kit (with optical module)

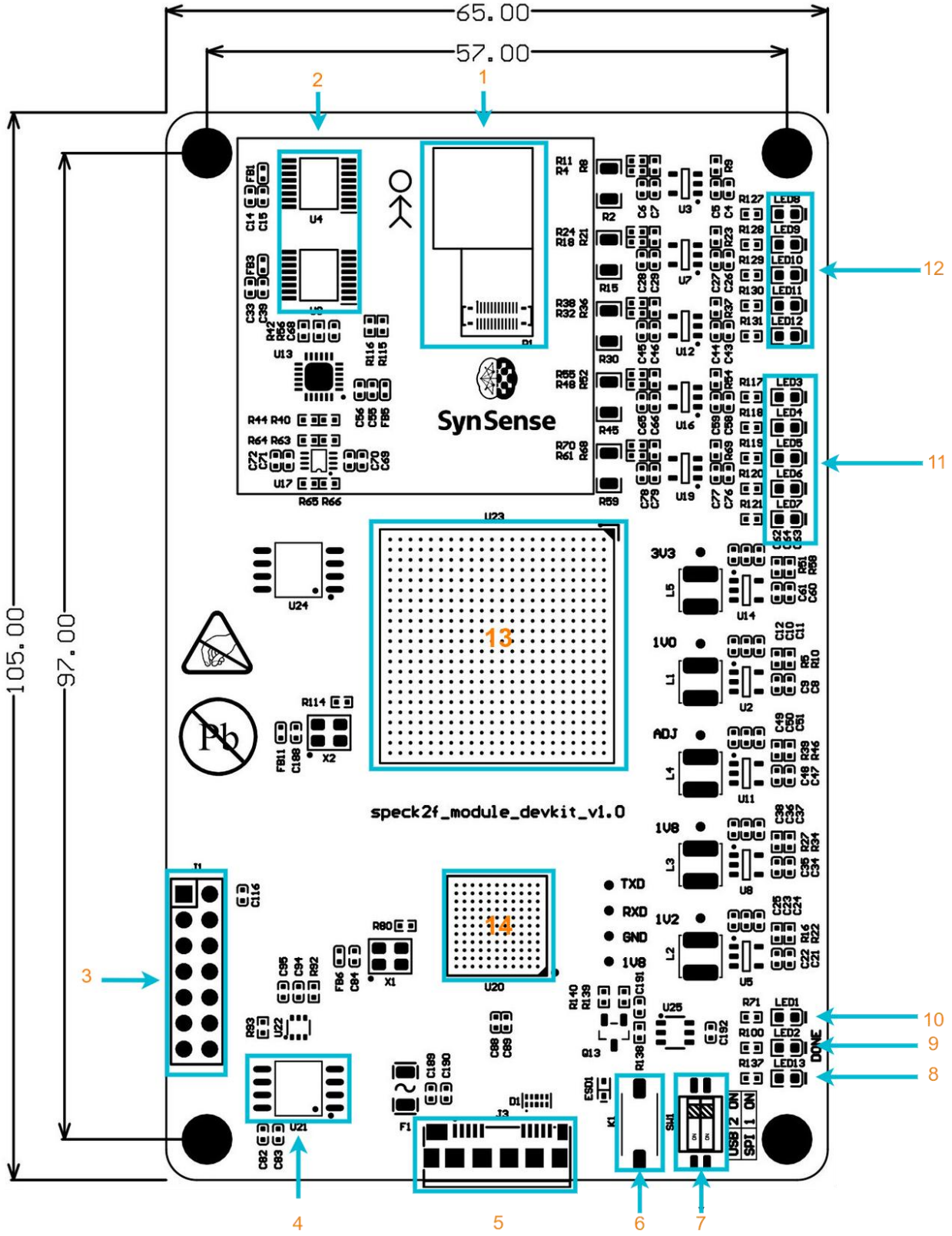


Figure 4 . Front view of the Speck™ dev kit (with optical module) (mm)

1. Speck™ Optical Module
2. High Precision Power Monitor
3. FPGA JTAG (RSV)
4. Flash
5. USB 3.0 Micro-B Port
6. System Reset Button
7. USB 3.0 Controller CFG Switch (RSV)
8. System Power LED
9. FPGA CFG Done Indicator
10. USB 3.0 Controller State Indicator
11. Debug State Indicator
12. SoC Power Traces State Indicator
13. FPGA
14. USB 3.0 Controller

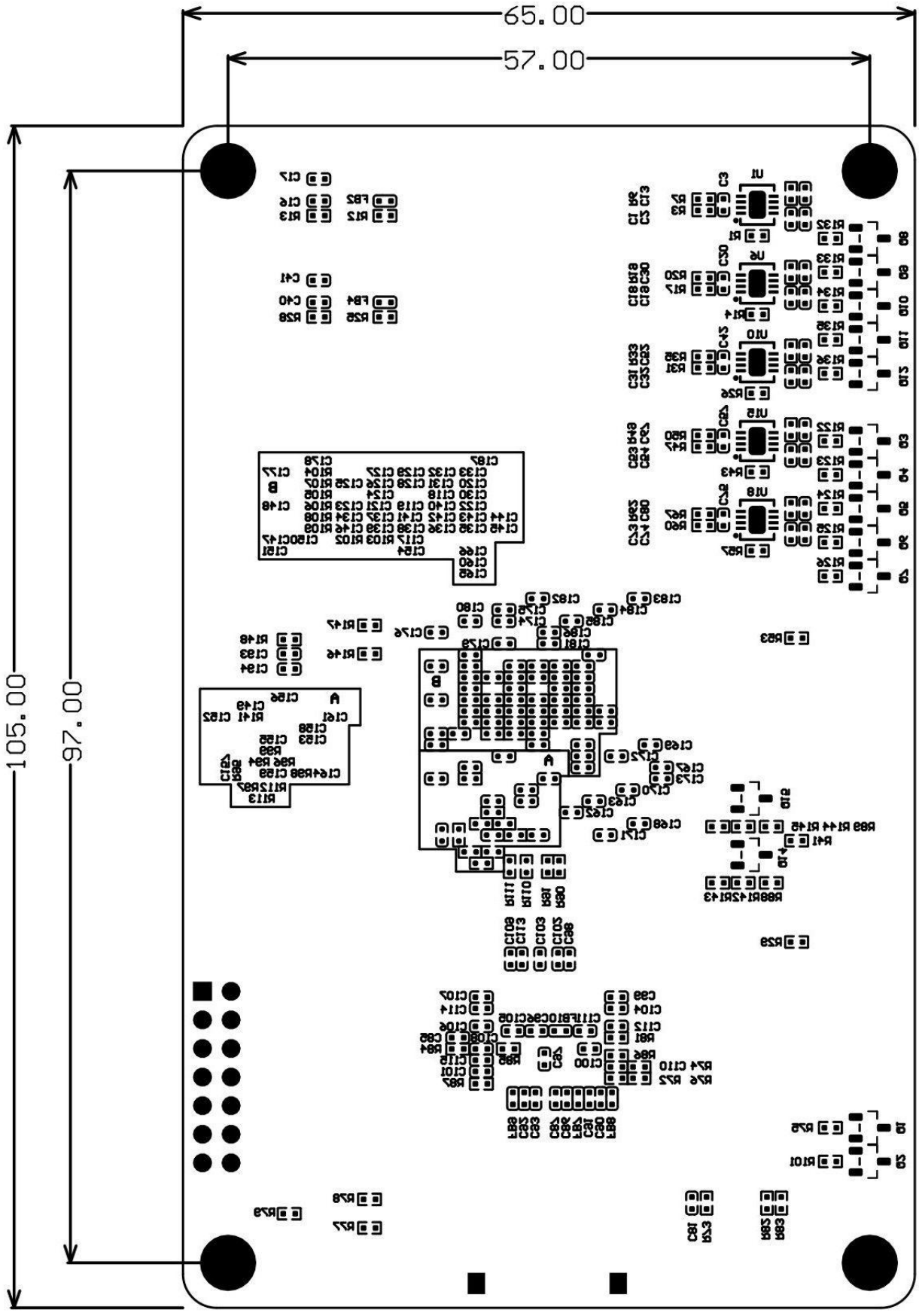


Figure 5 . Back view of Speck™ dev kit (with optical module) (mm)

4. Speck™ specification

4.1. Block diagram

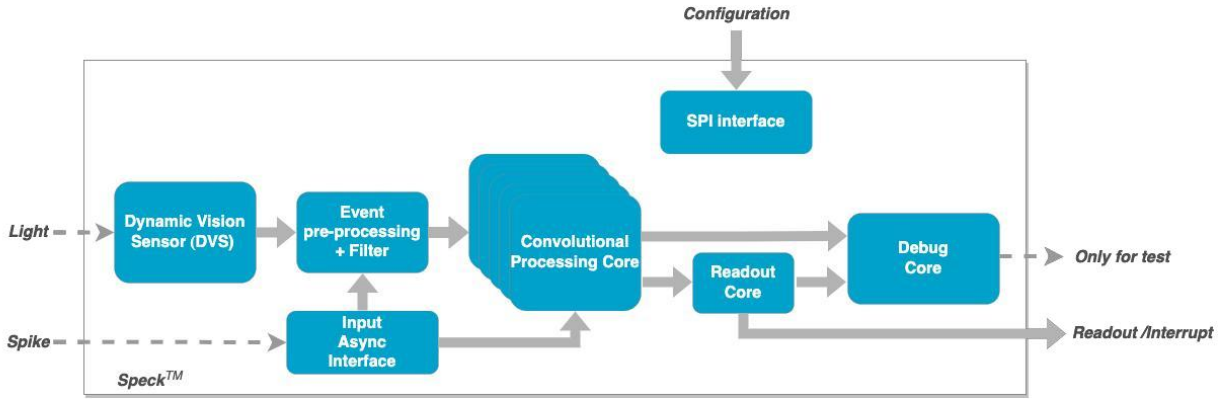


Figure 6 . Speck™ block diagram

4.2. DYNAP™-CNN convolutional computing layers

Speck™ is equipped with 9 configurable spiking convolutional computing layers. The layers can each implement a layer of a SCNN neural network, and can be connected to form a user defined network of any size up to the maximum available resources. Layer memory sizes are balanced to provide a flexible balance of resources, with larger or smaller layers, in terms of kernel size or neuron number, as described in section 4.5.

4.3. Congestion balancer

In Speck™, each convolutional layer is equipped with a congestion balancer block at its data path input.

The congestion balancer enables dropping of input spikes at any time when the convolutional core of the layer is busy processing previous data. Specifically, if a train of spikes are sent to the layer, a number of them will be accepted (via some buffering) and the convolution computation starts. If, for example, the kernel is very large and a new spike arrives while the layer input is busy, this new spike will be dropped. As soon as the layer is again available, a coming spike will be processed.

This block is then able to adapt the spike input frequency to the convolution by capping it to the maximum that the layer can process. When disabled, the block will let all spikes through.This feature is controlled by the input_congestion_balancer_enable.

4.4. Spike decimator

In Speck™, each convolutional layer is equipped with a decimator block at its data path output. The decimator block enables the user to reduce the spike rate at the output of a convolutional layer. When disabled, the block will let all spikes through.
This feature is controlled by the output_decimator_enable.

4.5. Memory capacity

The Speck™ is divided into 9 cores, each of which executes a single CNN layer. The memory capacities of the cores are different, and restrict the implementation of larger layers to specific cores.

Core.	Kernel memory (WORD)	Leak memory (WORD)	Neuron memory (WORD)
0	16 Ki	1 Ki	64 Ki
1	16 Ki	1 Ki	64 Ki
2	16 Ki	1 Ki	64 Ki
3	32 Ki	1 Ki	32 Ki
4	32 Ki	1 Ki	32 Ki
5	64 Ki	1 Ki	16 Ki
6	64 Ki	1 Ki	16 Ki
7	16 Ki	1 Ki	16 Ki
8	16 Ki	1 Ki	16 Ki

SRAM	Filter memory (WORD)
DVS Filter	16 Ki

	Memory Type	Word Length
1	Kernel	8 bits
2	Neuron	16 bits
3	Leak	16 bits
4	Filter	16 bits

Let a network be defined by the number of input features c, the number of output features f, and the kernel dimensions k_x and k_y.

The theoretical number of WORDs required for kernel memory K_M is then

$$K_M = cf\,k_x\,k_y$$

The total number of memory WORDs required is

$$K_{MT} = c \cdot 2^{\lceil \log_2(k_x k_y) \rceil + \lceil \log_2(f) \rceil}$$

The required number of neuron memory WORDs NM depends on the dimensions of the input features c_x and c_y, as well as the stride and padding s_x, s_y, and p_x, p_y.

$$f_x = \frac{c_x - k_x + 2p_x}{S_x} + 1$$

$$f_y = \frac{c_y - k_y + 2p_y}{S_y} + 1$$

$$N_M = f\,f_x\,f_y$$

Again the total number of required WORDs on the chip side is larger.

$$N_{MT} = f \cdot 2^{\lceil \log_2(f_y) \rceil + \lceil \log_2(f_x) \rceil}$$

4.6. Readout layer

The main use of the post-processing block is to calculate the moving average over a time window for a maximum of 15 neurons, provide the maximum average of the 15 neurons and compare the value of the calculated moving averages against a specified threshold. 5 pins of Speck™ are dedicated to the direct readout of the class of maximum activity, these pins (INTERRUPT and READOUT1 to 4) are designed to provide a direct

readout of the maximum spiking class (with or without activity threshold).

4.6.1 Interrupt

This pin outputs 0 until the class of max activity exceeds the threshold. Alternatively, the threshold comparison can be overridden by setting override_threshold_max to True. In this case, INTERRUPT becomes 1 at every falling edge of the slow_clk.

The INTERRUPT pin is raised at the falling edge of the slow_clk only if override_threshold_max is True or the max class activity is again above the selected threshold.

4.6.2 Readout pins

There are 4 readout pins. READOUTx pins reflect the index of the class of max activity as described in Data Output Modes. These pins are activated in two cases:

- A class has spiked more than the set threshold during the previous readout clock period (INTERRUPT is also raised when this condition is met).
- The override_threshold_max is set to True (override threshold).

The 4 bits reflect the binary value of the most recent spiking class. As such, in an application requiring only 4 classes, the CNN can be configured such that the four output classes are encoded as class 1, 2, 4 and 8 when arriving at the readout layer. In this condition, the 4 output pins READOUTx will each directly reflect one of the classes of interest, and no decoder will be needed to interpret the chip output.

4.7. Others

For a more detailed explanation of the reading principle and method for the Speck™ chip output, as well as instructions for configuring and utilizing the on-chip CNN and other resources, please contact technical support or visit SynSense's publicly available materials on GITLAB.

5. Getting started

SynSense provides Tonic, Sinabs and Samna to help development on the Speck™ dev kit (with optical module).

Tonic provides publicly available event-based vision and audio datasets and event transformations. The package is fully compatible with PyTorch Vision/Audio to give you the flexibility that you need. It caters to both the event-based world that works directly with events or time surfaces as well as to more conventional frameworks which might convert events into dense representations in one way or another.

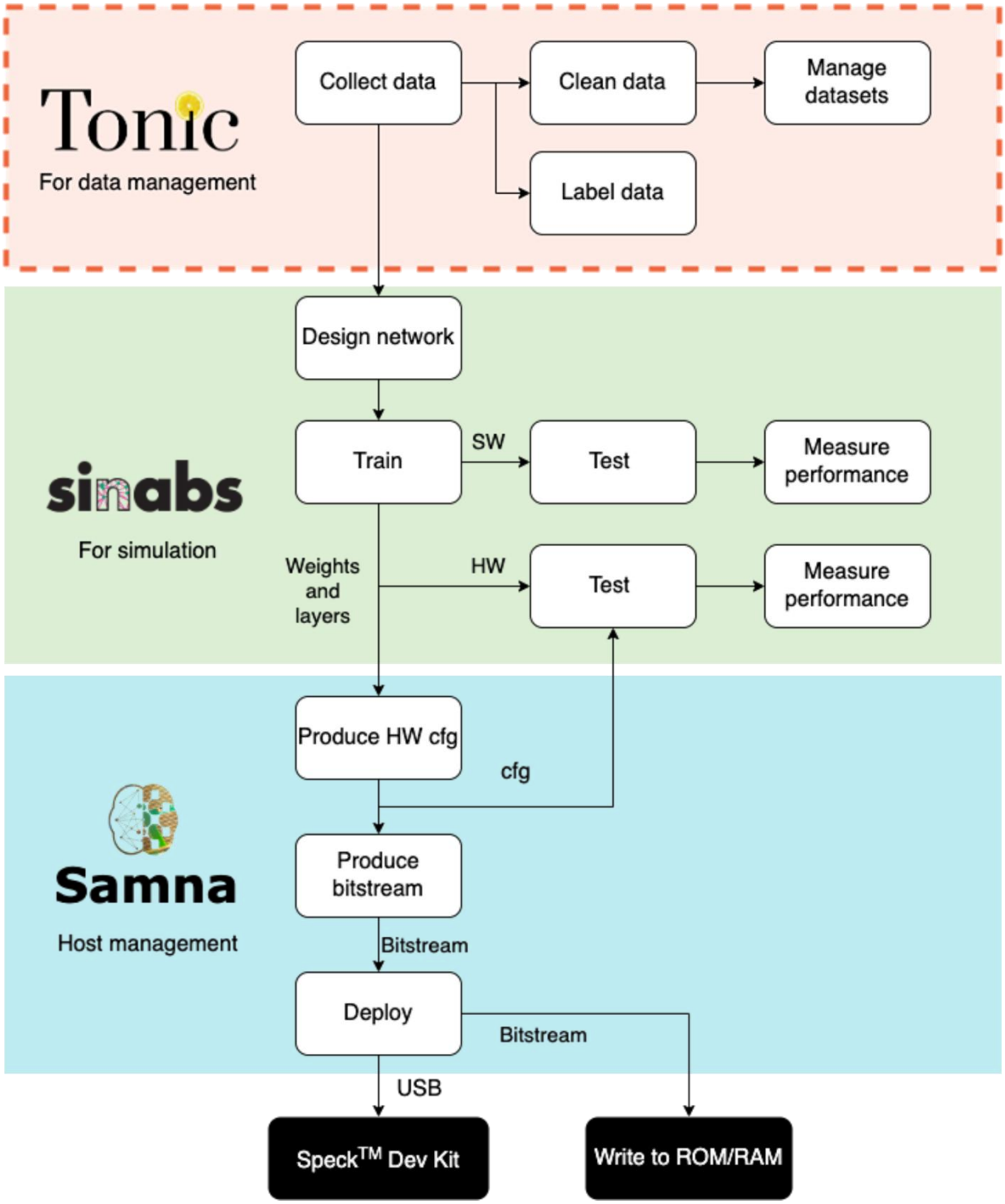
Sinabs is a Python library for development and implementation of Spiking Convolutional Neural Networks (SCNNs). The library implements several layers that are spiking equivalents of CNN layers. In addition it provides support to import CNN models implemented in torch conveniently to test their spiking equivalent implementation.

Samna is the developer interface to the SynSense toolchain and run-time environment for interacting with our devices. Written in C++, it provides a Python API and data visualization tools for working with spiking neural networks and for processing streams of event-based data.

An SNN model developed in Sinabs can be easily deployed onto the Speck™ dev kit (with optical module) with the help of Samna.

It is possible to connect an external DVS camera to the board, more info can be found at Send events from a DVS to a dev kit using a graph.

For more examples please refer to Samna official documentation.


Tonic
For data management
Collect data
Clean data
Manage datasets
Label data
sinabs
For simulation
Design network
Train
SW
Test
Measure performance
Weights and layers
HW
Test
Measure performance
Samna
Host management
Produce HW cfg
cfg
Produce bitstream
Bitstream
Deploy
Bitstream
USB
Speck™ Dev Kit
Write to ROM/RAM

6. Readout pin monitoring

The readout layer in Speck™ is the post-processing layer, the output results are readable through the 4 readout pins if an interrupt happens if configured correctly. Using the readout pin monitoring feature provided by the dev kit, it is possible to validate your model close to real application scenarios.

The readout pin monitoring feature can be enabled via Samna. To enable the readout layer, the samna.speck2f.configuration.ReadoutConfig.enable needs to be set to True first. To forward your model's last layer to the readout layer, you need to set its destination to 12.

The samna.speck2f.configuration.ReadoutConfig.readout_configuration_sel needs to be set according to your model. There are 4 different addressing modes that could be selected:

Value	Mode
0	2x*2y*4f
1	2x*4y*2f
2	4x*4y*1f
3	1x*1y*16f

And set the samna.speck2f.configuration.ReadoutConfig.threshold of the readout layer according to your model. The moving average of the output neurons is compared to the threshold value to produce an output if the received number of spikes is greater than the threshold.

The Speck™ readout layer also provides a low pass filter. There are two selectable time windows, 16 (16 * slow clk period) and 32 (32 * slow clk period), which can be chosen by samna.speck2f.configuration.ReadoutConfig.low_pass_filter32_not16. The default value is False, which is 16 * slow clk period. The low pass filter is **enabled by default**, if you don't want to use it, please set samna.speck2f.configuration.Readout-Config.low_pass_filter_disable to True.

Then we set samna.speck2f.configuration.ReadoutConfig.readout_pin_monitor_enable to True in order to monitor the 4 readout pins. If there is a valid result, an interrupt is generated by the chip and a samna.speck2f.event.ReadoutPinValue event is sent to Samna. The samna.speck2f.event.ReadoutPinValue contains 2 members, an index, indicating the feature, and a timestamp in microsecond, indicating when this event happened.

Note: *Speck2f.* is the software developed for this dev kit, and will be supported through the update of Samna.

7. On board power monitor

The Speck™ dev kit (with optical module) comes with on board power monitor capability for the five power races of Speck™ through Samna: VDD_IO, VDD_RAM, VDD_LOGIC, VDD_PIXEL_DIGITAL, VDD_PIXEL_ANALOG, which are represented by channel 0, 1, 2, 3, 4 respectively.

```
import samna
import time
d = samna.device.get_unopened_devices()
dk = samna.device.open_device(d[0])

power = dk.get_power_monitor()
buf = samna.BasicSinkNode_unifirm_modules_events_measurement()
graph = samna.graph.EventFilterGraph()
graph.sequential([power.get_source_node(), buf])
graph.start()

print("Manual power monitor test:" )
power.single_shot_power_measurement()
time.sleep(1)
ps = buf.get_events()
[print(p) for p in ps]
time.sleep(2)

print("Auto power monitor test:" )
# set freq to 1 Hz. The maximum power monitor rate is 100 Hz
power.start_auto_power_measurement(1.0)
time.sleep(5)
power.stop_auto_power_measurement()
ps = buf.get_events()
[print(p) for p in ps]
```

Note: The on board power monitor has about ± 50uW offset on each power trace. Max sampling rate 100Hz.

8. Appendix

8.1. Declaration of Non-Ideal Scenarios and Influencing Factors

The Speck™ chip integrates a Dynamic Vision Sensor (DVS) and a dedicated neuromorphic vision processing core (DYNAP™CNN) on-chip. The input of the entire chip system is light, and the illumination conditions directly and greatly affect, interfere with, or even damage the device's operating status. The main external factors are illuminance and flicker. In addition, like many other sensors, especially RGB sensors, dirt on the lens, smoke, fog, or direct obstruction in the scene can also affect or disrupt the normal execution of the system's application. Furthermore, extreme (high or low) temperatures can also affect or even damage the normal operation of the silicon-based chip.

8.1.1 Illumination

All sensors produce both signals and noise at the same time. For light-dependent sensors such as Dynamic Vision Sensors (DVS), the signal (valid event) is greatly reduced under low illumination, and the background noise increases. While the target action contour may be vaguely visible to the naked eye, it presents a significant challenge for algorithm models. In fact, all major DVS manufacturers currently have a very wide dynamic range for on-chip Dynamic Vision Sensors (DVS) measured in the laboratory, theoretically supporting imaging at very low illumination levels. However, in this case, the effective "events" are too sparse to effectively support application requirements.

The dynamic vision sensor (DVS) integrated in the Speck™ chip by SynSense Technology is capable of supporting imaging under lighting conditions as low as 10 lux, according to data obtained in the laboratory. However, in typical application scenarios, it has been found:

- In a 10~20 lux environment, the current application algorithm model performance shows a significant decrease.
- In scenes with 20-50 lux lighting conditions, there is a slight increase in delay in the application algorithm model, which may result in missed or erroneous judgments (<5%);
- In scenes with lighting conditions greater than 50 lux, the application algorithm model works stably and produces highly reliable results (>95%);

China National Illumination Standards (excerpted).

Residential Building Lighting Standards		
Room or Area	**Reference Plane and Height**	**Illumination Standards (lx)**
Living Room (General Activity)	0.75m Horizontal Plane	100
Living Room (Writing, Reading)	0.75m Horizontal Plane	300
Bedroom (General Activity)	0.75m Horizontal Plane	75
Bedroom (Writing, Reading)	0.75m Horizontal Plane	150
Dining Room	0.75m Table Surface	150
Kitchen (General Activity)	0.75m Horizontal Plane	100
Kitchen (Operation Table)	Table Surface	150
Bathroom	0.75m Horizontal Plane	100
Note: Mixed lighting is recommended.		

Commercial Building Lighting Standards		
Room or Area	**Reference Plane and Height**	**Illumination Standards (lx)**
General Store	0.75m Horizontal Plane	300
High-End Store	0.75m Horizontal Plane	500
General Supermarket	0.75m Horizontal Plane	300
High-End Supermarket	0.75m Horizontal Plane	500
Cashier Desk	Table Surface	500

Library Building Lighting Standards		
Room or Area	**Reference Plane and Height**	**Illumination Standards (lx)**
General Reading Room	0.75m Horizontal Plane	300
National, Provincial and Other Important Libraries' Reading Room	0.75m Horizontal Plane	500
Elderly Reading Room	0.75m Table Surface	500
Rare Books and Documents Reading Room	0.75m Horizontal Plane	500
Exhibition Hall, Catalog Hall, Cashier's Hall	0.75m Horizontal Plane	300
Bookstacks	0.25m Horizontal Plane	50
Workspace	0.75m Horizontal Plane	300

Office Building Lighting Standards		
Room or Area	**Reference Plane and Height**	**Illumination Standards (lx)**
General Office	0.75m Horizontal Plane	300
High-Grade Office	0.75m Horizontal Plane	500
Conference Room	0.75m Table Surface	300
Reception Desk, Front Desk	0.75m Horizontal Plane	300
Sales Hall	0.75m Horizontal Plane	300
Design Room	Actual Work Surface	500
Document Organization, Copying and Distribution Room	0.75m Horizontal Plane	300
Data Archive Room	0.75m Horizontal Plane	200

Lighting Standards for School Buildings		
Room or Area	**Reference Plane and Height**	**Illumination Standards (lx)**
Classroom	Desk surface	300
Laboratory	Laboratory table surface	300
Art room	Table surface	500
Multimedia classroom	0.75m above horizontal plane	300
Classroom blackboard	Blackboard surface	500

Lighting Standards for Hospital Buildings		
Room or Area	**Reference Plane and Height**	**Illumination Standards (lx)**
Treatment room	0.75m above horizontal plane	300
Laboratory	0.75m above horizontal plane	500
Operating room	0.75m above horizontal plane	750
Consulting room	0.75m above horizontal plane	300
Waiting room, registration hall	0.75m above horizontal plane	200
Ward	Floor surface	100
Nurse station	0.75m above horizontal plane	300
Pharmacy	0.75m above horizontal plane	500
Intensive care unit	0.75m above horizontal plane	300

Lighting Standards for Public Places		
Room or Area	**Reference Plane and Height**	**Illumination Standards (lx)**
Lobby (ordinary)	Floor surface	100
Lobby (luxury)	Floor surface	200
Corridors and passageways (ordinary)	Floor surface	50
Corridors and passageways (luxury)	Floor surface	100
Stairs and platforms (ordinary)	Floor surface	30
Stairs and platforms (luxury)	Floor surface	75
Escalators	Floor surface	150
Toilets, bathrooms (ordinary)	Floor surface	75
Toilets, bathrooms (luxury)	Floor surface	150
Elevator lobby (ordinary)	Floor surface	75
Elevator lobby (luxury)	Floor surface	150
Rest room	Floor surface	100
Storage room, warehouse	Floor surface	100
Garage (ordinary)	Floor surface	75
Garage (luxury)	Floor surface	200
Note: The lighting standards for power stations and substations in residential and public buildings shall be selected from the table.		

8.1.2 Flicker

- Like all light-based sensors, the Dynamic Vision Sensor (DVS) integrated within the Speck™ chip is also sensitive to low-frequency "on/off" flickers of light. From the imaging principle of the DVS, for low-frequency flickers, effective "events" can be easily overwhelmed by flicker noise.
- The Speck™ chip can operate normally under the power frequency flicker conditions that comply with the GB/T31831 "LED Indoor Lighting Technology Application

Requirements" national standard. For power frequency flicker exceeding the national standard, the integrated anti-flicker filter in the Speck™ chip can be enabled to optimize the on-chip power frequency filter. However, due to the complex types of power frequency flicker scenarios that exceed the national standard, the built-in anti-flicker filter cannot completely eliminate/effectively suppress all non-national standard flickers.

- In practical applications, as long as the main light source does not have flicker frequency bands or flicker depth beyond the national standard, ambient light will not cause significant interference or damage to the application model of Speck™. In other words, Speck™ and the application algorithm model itself can tolerate some minor flickers (flicker frequency and depth of direct and reflected light from the target) of secondary light sources in the application scenario that exceed the national standard (low-risk area, see Chapter 8.2).

8.1.3 Obstruction, Smoke and Fog

- Obstruction can affect the integrity of imaging and directly damage the correct execution of algorithmic models.
- Mild smoke and fog can be tolerated by the applied algorithmic model, but dense smoke or fog is like the lens being obstructed.

8.1.4 Extreme temperatures

- The dynamic visual sensor (DVS) integrated on the Speck™ chip contains a large number of analog circuits that are temperature-sensitive. If the temperature exceeds the application scenarios supported by the manufacturer, it will directly lead to partial loss of the imaging function of the DVS, and in severe cases, it will directly fail.
- The production of the Speck™ optical module is similar to that of the RGB optical module. Considering the production process of the module, it is also not suitable for use under temperature conditions beyond the support range. Currently, the Speck™ chip and optical module can be used in an environment of 0-65°C, and it is strongly recommended to use it in a scene of 15-65°C to ensure more stable DVS imaging.

8.2. Non-standard flicker

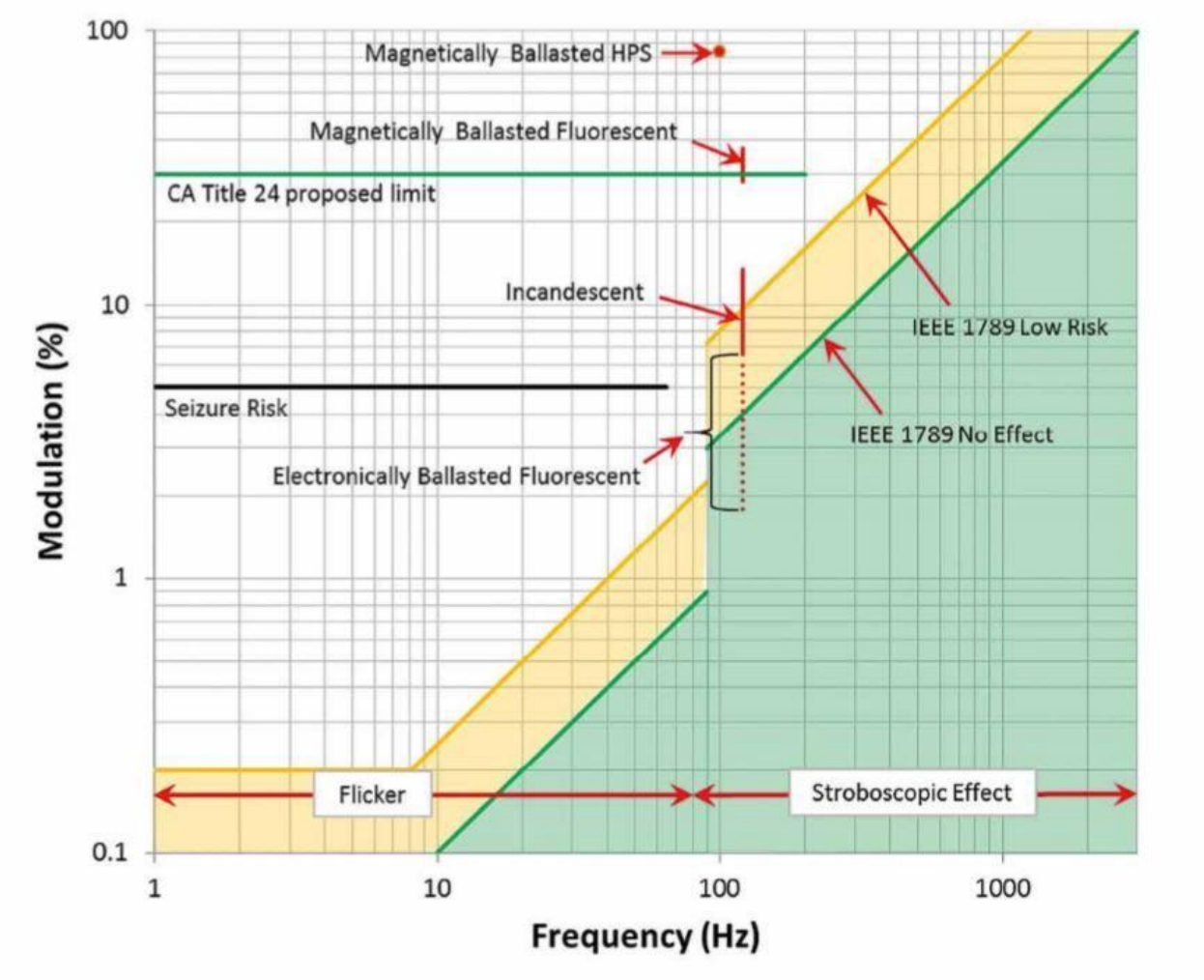


Figure 7 . IEEE 1789 'Recommended Practices' for Light Flicker

According to the domestic GB/T31831 document "Application Requirements for LED Indoor Lighting Technology", the harmless limit of flicker percentage for lamps is specified in the table below:

Flicker Percentage (Flicker Depth) Requirements for Low-Risk	
Flicker (Modulation) Frequency f	**Flicker Percentage (FPF) Limitation Value %**
<8Hz	FPF≦0.2
8 - 90HZ	FPF≦0.025 × f
90 - 1250Hz	FPF≦0.08 × f
>1250Hz	Low-risk exemption

According to the domestic GB/T31831 document "Application Requirements for LED Indoor Lighting Technology", the harmless limit of flicker percentage for lamps is specified in the table below:

Flicker Percentage (Flicker Depth) Requirements for Harmless	
Flicker (Modulation) Frequency f	**Flicker Percentage (FPF) Limitation Value %**
10 - 90HZ	FPF≦0.01 × f
90 - 3125Hz	FPF≦0.08 × f / 2.5
f >3125Hz	High-frequency exemption

9. Change log

No.	Ver	Date	Editor	Changes
1	V0.1	2023.04	SI	Initial version
2	V0.2	2023.06	SI	Update power measurement example code

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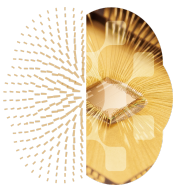

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