# Speck™

## Optical Module User Guide Feb 2025

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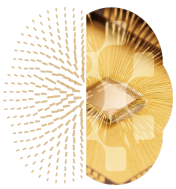

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# Contents

# 1. Overview

This user guide describes the basic specifications, hardware information, and basic usage of the optical module SYNS91105M.

Number: SYNS91105M

Number of built-in pulse neurons: 320,000

Built-in DVS* Resolution: 128x128 128x128

DVS target aspect ratio: 1:1

Data interface: GPIO + interrupt + SPI (master/slave)

Connector: BM28B0.6-24DP BM28B0.6-24DP/2-0.35V(51)

Optical specifications 3.62mm/1.98mm lens

Size: 18.5x9.75x4.98mm/18.5x9.75*3.68mm

Description DVS*, Dynamic Vision Sensor, also known as event-based camera, event camera. The optical module SYNS91105M based on Speck™ can be used in the following application scenarios, including but not limited to the following areas:

- Smart toys,
- Smart home,
- Smart Cockpit,
- Drones, Unmanned Vehicles,
- Computers, mats Peripherals,
- Live and recorded broadcasting, etc.

# 2. About Speck™

In the context of the traditional AI encountering bottlenecks in computational power and energy consumption, neuromorphic computing, through the inspiration from the operating mechanisms and cognitive behaviors of the biological brain, is expected to bring new exploration paths for the further development and practical application of artificial intelligence technology. By adopting bio-inspired asynchronous circuit design, the high power consumption defects brought by clock-based traditional synchronous circuit design are eliminated. As a key part of the neuromorphic intelligence system, these unique technological advantages of the neuromorphic chip greatly enhance the utilization rate of hardware resources and the operational efficiency of pulse neural networks.

Speck™ is the world's first "sensor-compute integrated" neuromorphic intelligent dynamic vision SoC, integrating an asynchronous neuromorphic dynamic vision processor (DYNAP™CNN) and a Dynamic Vision Sensor (DVS), also known as an Event Camera, Dynamic Event-based Sensor (DES), or Event-based Vision Sensor (EVS). It features a large-scale spiking convolutional neural network (sCNN) chip architecture based on an asynchronous logic paradigm, configurable with up to 320,000 spiking neurons, and internally integrates the state-of-the-art event-based, 128x128 resolution dynamic vision sensor (DVS) for real-time and efficient dynamic vision input.

Speck™ paves the way for always-on IoT devices and applications such as edge computing and human-machine interaction, behavior recognition, gesture recognition, facial detection, human tracking, and surveillance, with ultra-low power consumption and ultra-low latency.

## 2.1. Speck™ SoC chip features

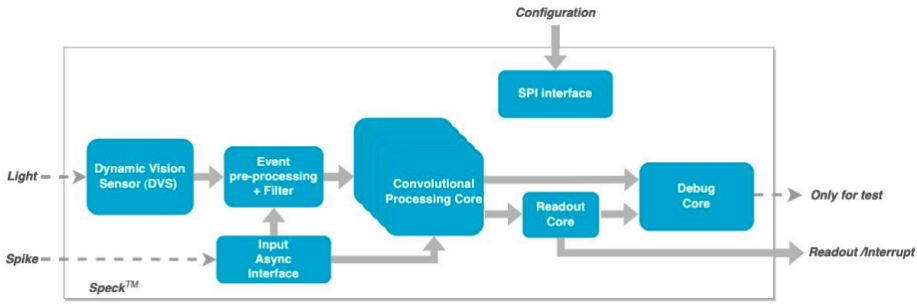



Figure 1 . Block diagram of internal functions(A)

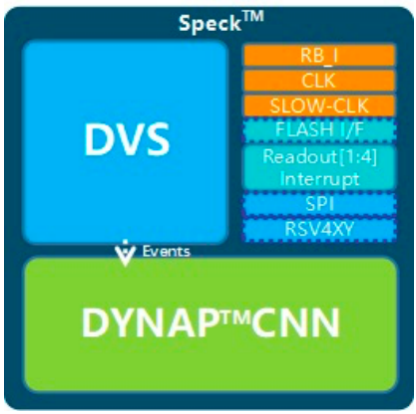



Figure 2 . Block diagram of internal functions(B)

### 2.1.1 Key features

- 1 Built-in DVS layer
- 9 DYNAP™CNN layer
- 1 Readout layer
- SPI slave/master instarface
- Sum pooling {1:1, 1:2, 1:4}
- Fanout of 2
- Ultra-low average working power consumption

### 2.1.2 DVS layer

- 128x128 array
- Noise filtering

- DVS polarity adjustment
- ROI selection
- Mirroring in both X/Y
- Rotate in 90-degree steps
- Dynamic range not less than 80 dB (20-200k lux)

**Note**: When used between 20lux to 50lux, there is a slight decrease in the sensitivity of the optical sensor array, and there may be a slight increase in the delay of the algorithm model. There is a possibility of occasional missed or erroneous judgments (with a probability of less than 5%, see Chapter 8.1 in the appendix).

### 2.1.3 DYNAP™-CNN computing layers

- Up to 9 CNN layers
- Max input dimension 128*128
- Max feature output size 64*64
- Max feature number 1024
- Weight resolution 8 bits
- Neuron state resolution 16 bits
- Max kernel size 16*16
- Stride {1,2,4,8} independent in X/Y
- Padding [0..7] independent in X/Y
- Pooling 1: 1, 1:2, 1:4
- Fanout of 2
- Leak operation on each layer
- Spike decimator on each layer
- Spike congestion balancer on each layer
- Parallel computing on layer 0 and layer 1, enabling larger throughput, can be used as input layers

### 2.1.4 Readout layer

- 15 classes and 1 idle class
- Selectable moving average between 1, 16 and 32 time steps.
- 4 readout modes: inactive/threshold/max spiking class/specific class.
- 4 readout pins and 1 interrupt pin

### 2.1.5 Package

- COB

## 2.2. Application scenario

Speck™ is a pioneering combination of dynamic vision sensing and event-driven computing, providing a highly real-time, integrated and low-power dynamic vision solution. In typical application scenarios, Speck™ can complete intelligent scene analysis with ultra-low power consumption and real-time response:

- Event classification
- Behavior detection
- Pattern recognition
- Visual wake-up/detection
- Gesture recognition for IoT interaction or control applications
- Facial attention monitoring
- Ultra-low power edge computing
- Smart device control
- Security/safety monitoring, etc.
- Functionality schematic

# 3. Speck™ Optical Module

SYNS91105M optical module is prepared as a general-purpose SpeckTM module by combining SpeckTM2 chip based on COB package, supplemented with necessary hardware design and configured with lenses (3.62mm here) according to the typical application requirements; as a standardized module and complete brain-like intelligent dynamic vision solution, it supports direct interface with necessary peripherals or other processors through a 24pin B2B connector, which greatly reduces the workload of hardware and software and system cost in product development and accelerates the time-to-market of customers' products. As a standardized module and complete dynamic vision solution, it supports a 24-pin B2B connector to directly interface with necessary peripherals or other processors to complete the information transfer, data interaction or output of calculation results, which greatly reduces the workload and system cost of hardware and software in product development, and accelerates the time to market of customers' products.

Figure 3 . Front view of Speck™ module

## 3.1. Module diagram

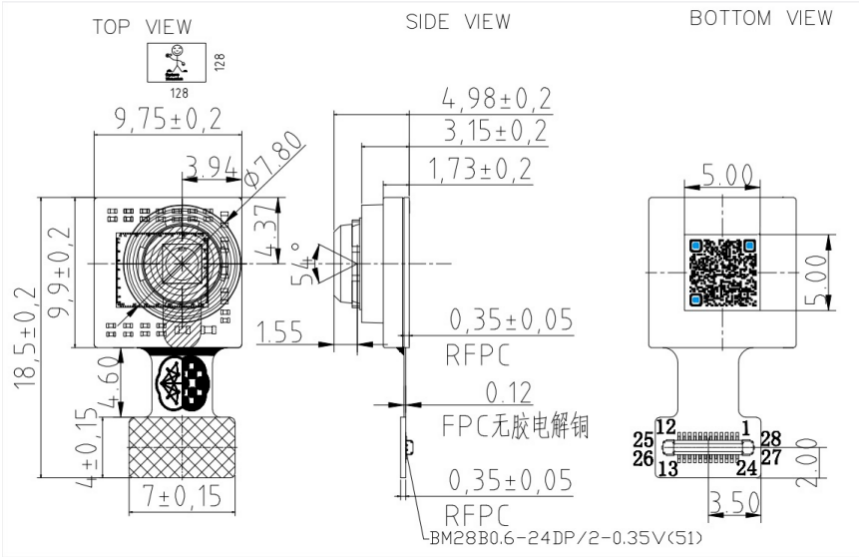



Figure 4 . Size of the 3.62mm lens

## 3.2. 3.62mm optical module specification

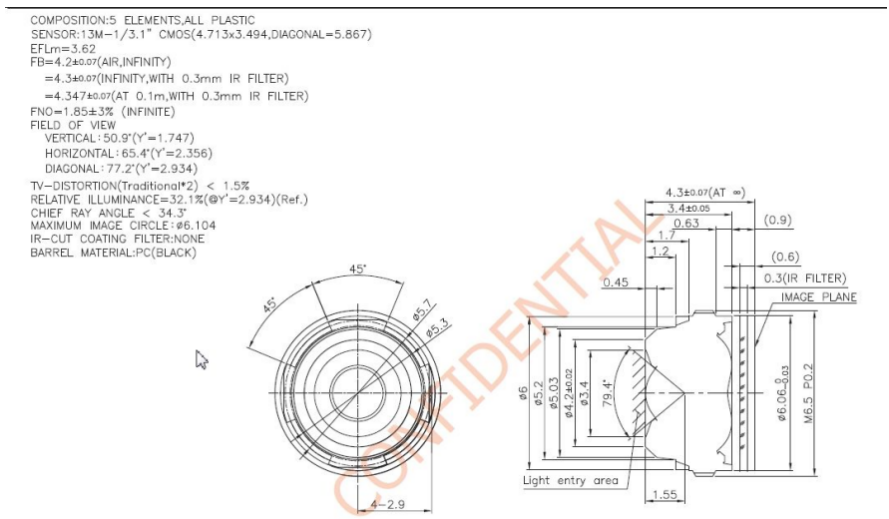



Figure 5 . Specification of the 3.62mm lens

The quick calculation formula for the field of view angle of a DVS sensor under different focal length lenses is:

HFOV = 2 * ARCTAN(H / (2 * EFL)), VFOV = 2 * ARCTAN(V / (2 * EFL))

For example, the H-FOV of SYNS91105M (3.62mm) is 38.95°, and the V-FOV is also 38.95°. (Here, H = V = 2.56mm, EFL is the focal length of the lens (3.62mm), H-FOV is the horizontal field of view angle, and V-FOV is the vertical field of view angle).

Note: SynSense has released another 1.98mm lens version of the optical module (please refer to Appendix 8.5). For other specifications, please contact SynSense.

## 3.3. Module interface

### 3.3.1 Connectors for modules

Model No.: BM28B0.6-24DP/2-0.35V(51)

Number of pins: 24

Pitch: 0.35mm

Number of rows: 2

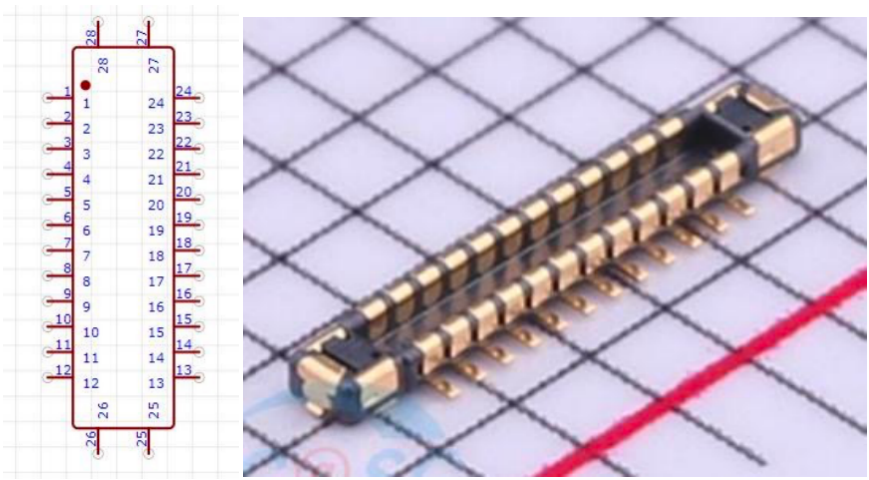


Figure 6 . Connector BM28B0.6-24DP/2-0.35V(51)

### 3.3.2 Connectors pin definition

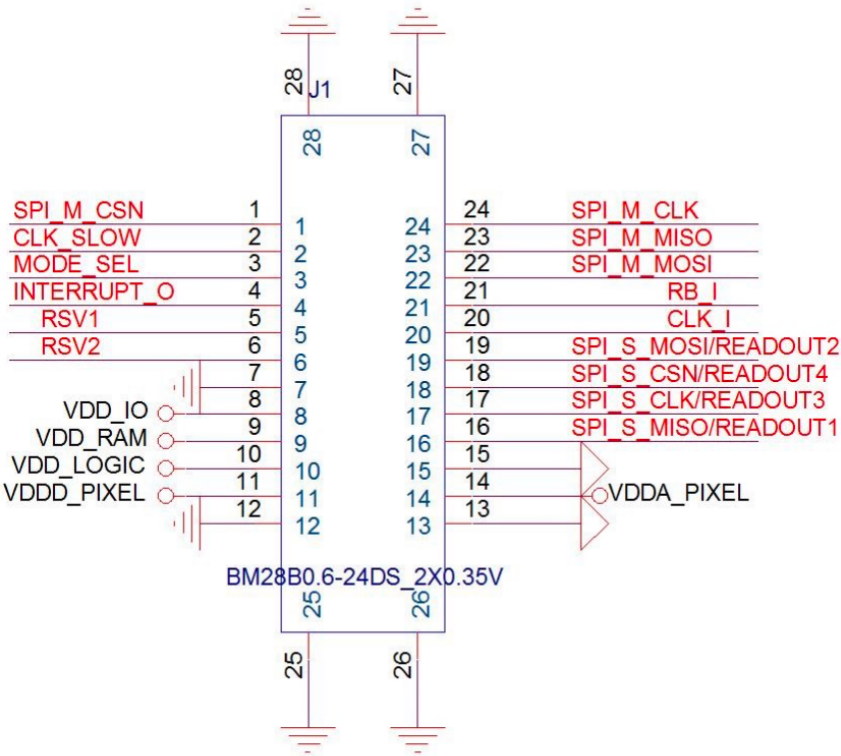



Figure 7 . Pin definition

### 3.3.3 Pin usage

| Pin No. | Pin Name | Usage |
|---|---|---|
| 1 | SPI_M_CSN | Input, SPI-master, to connect Flash or NC (when an external processor configures the chip via SPI-slave); |
| 2 | CLK_SLOW | Input to be used as a reference time window for READOUT; |
| 3 | MODE_SEL | Configuration Input, NCable |
| 4 | INTERRUPT_O | Output, chip valid output flag bit, can user wake up the external processor; |
| 5 | RSV1 | Reserved, NC (can be used for strobe detection by an external processor); |
| 6 | RSV2 | Reserved, NC |
| 7 | GND | GND |
| 8 | VDD_IO | Power input, chip IO power supply; |
| 9 | VDD_RAM | Power input, on-chip ram power supply; |
| 10 | VDD_LOGIC | Power input, on-chip logic power supply; |
| 11 | VDD_D_PIXEL | Power input , DVS array digital power supply; |
| 12 | GND | GND |
| 13 | GND | GND |
| 14 | VDD_A_PIXEL | Power input , DVS array digital power supply; |
| 15 | GND | GND |
| 16 | SPI__S__ MISO/READ OUT1 | Multi-function pin:<br>Can be used as output READOUT1 based on configuration parameter settings; also used as slave input, SPI_MISO;<br>Default priority is slave, SPI_MISO; |

| | | |
|---|---|---|
| 17 | SPI__S__CLK/READOUT3 | Multi-function pin:<br>Can be used as output READOUT3 based on configuration parameter settings; also used as slave input, SPI S CLK;<br>Default priority is slave, SPI_S_CLK. |
| 18 | SPI__S__CSN/READOUT4 | Multi-function pin:<br>Can be used as output READOUT4 based on configuration parameter settings; also used as slave input, SPI_CSN;<br>Default priority is slave, SPI_CSN. |
| 19 | SPI__S__MOSI/READOUT2 | Multi-function pin:<br>Can be used as output READOUT2 based on configuration parameter settings; also used as slave output, SPI_MOSI;<br>Default priority is slave, SPI_MOSI. |
| 20 | CLK_I | Input, reference clock source for interfaces such as chip SPI; |
| 21 | RB_I | Input, system reset, active low; |
| 22 | SPI_M_MOSI | Input, SPI-master, to connect Flash or NC (when an external processor configures the chip via SPI-slave); |
| 23 | SPI_M_MISO | Input, SPI-master, Flash connected or ground (when external processor configures the chip via SPI-slave); |
| 24 | SPI_M_CLK | Input, SPI-master, to connect Flash or NC (when an external processor configures the chip via SPI-slave); |
| 25-28 | GND or NC | Grounded, or NC |

# 4. Recommended Working Conditions

| Parameter | Description | Min | Type | Max | Unit |
|---|---|---|---|---|---|
| VDD_IO | IO power domain | 1.8 | 2.5 | 3.3 | V |
| VDD_RAM | On-chip distributed ram power domain | 1.1 | 1.2 | 1.3 | V |
| VDD_LOGIC | On-chip logic function power domain | 1.1 | 1.2 | 1.3 | V |
| VDD_D_PIXEL | DVS Array Digital Power Domain | 1.1 | 1.2 | 1.3 | V |
| VDD_A_PIXEL | DVS Array Analog Power Domain | 1.1 | 1.2 | 1.3 | V |
| Ta（TBD) | (Use) Ambient temperature | -15 | | 65 | ℃ |
| CLK | Reference clock for chip interface | 25 | 25 | 100 | MHz |

**Note:**

- The analog power supply of the DVS array, VDD A PIXEL, has a very light load and is very sensitive. It should be powered by a high-quality LDO and must not intersect with the ram or logic power supply; the PCB must be kept away from other power supplies and signals;
- The difference between the VDD A PIXEL and VDD D PIXEL supply voltages does not exceed 10%. For example, if VDD A PIXEL=1.1V, then VDD D PIXEL is not greater than 1.1V*110%=1.21V.
- The ram and logic power supply of the chip has light load, so it is recommended to use LDO for supply;
- The supply quality of each power rail (VDD_RAM/VDD_LOGIC/VDD D PIXEL/VDD A PIXEL) in the chip should be paid attention to and should not exceed the voltage range specified in the table. In addition, for better component life and performance, the recommended voltage working range is 1V2±5%;
- The chip IO (VDD_IO) supports a wide voltage range of 1V8~3V3. The chip system consumes less power at 1V8 and has the best performance at 2V5;

- The chip power-on sequence is: first reset the chip (RB_I is set low), then VDD_IO is supplied before other power supplies in the chip, or several power rails in the chip are supplied at the same time; until it is confirmed that each power supply meets the supply requirements, the reset signal is released (set high ); During normal operation, RB_I should remain high;
- System reset signal RB_I, active low; when the reset takes effect (first set low, then set high), all chip configurations are cleared. At this time, the chip actively grabs the configuration from the external FLASH through the SPI-master; when there is no external FLASH, external processing The device can download configuration to the chip through SPI-slave. It can be set to power-on reset off-chip, and the time is greater than 1us; it is recommended that an external processor handle the reset management of the chip;
- CLK serves as the reference clock source for chip SPI and other interfaces, and is recommended to be 25Mhz;
- The effective output pins of the chip are Interrupt_O+READOUT[1:4].

# 5. Hardware Usage

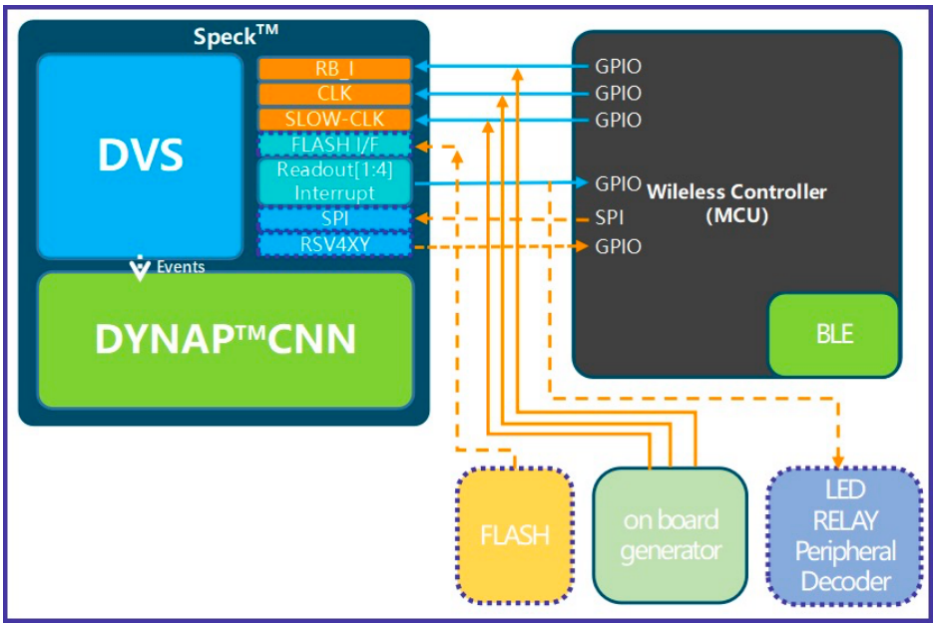



Figure 8 . Hardware usage diagram

- According to the chip power-on sequence requirements, during the system power-on process, the chip should be reset (RB_I is "low"); power on the IO first, then power on the DVS (sensor) and NPU (DynapTMCNN Processor core), or they can be powered on at the same time. Power on VDDIO and VDD_RAM/VDD_LOGIC of the NPU part and VDD_D_PIXEL/VDD_A_PIXEL of the sensor part; after confirming that the chip is powered on, release the reset (RB_I remains "high"), and then configure the SpeckTM chip;
- After reset and power-up, the SpeckTM chip can automatically grab the configuration file stored in the external flash via the SPI_master interface (pin22--24 of the module, pin1) (when SPI_M_CLK = 25Mhz, the configuration takes about 200mS); or the external processor can configure the SpeckTM chip via the SPI--SLAVE interface (pin16--19 of the module) (the time consumed is dependent on the maximum effective SPI_CLK rate supported by the external processor).
- All input pins (including IOs multiplexed as SPI-slave pins) have been set up with default pull-down resistors (30k) inside the chip, so there is no need to give additional pull-up or pull-down resistors in use, otherwise the chip IO power consumption will be abnormal; if you have to add them, you should correctly set

certain register values to disable the on-chip default pull-down function of the IO;

**Note:** The off-chip processor should download the configuration to the SpeckTM chip via SPI-slave after the SpeckTM chip reset has taken effect for at least 1s, and SPI_M_MISO should be grounded to prevent false interference.

Based on the path/approach to configuring Speck$^{TM}$, 2 hardware reference circuits are listed here.

## 5.1. Speck$^{TM}$ self-starting, grabbing configuration from external flash

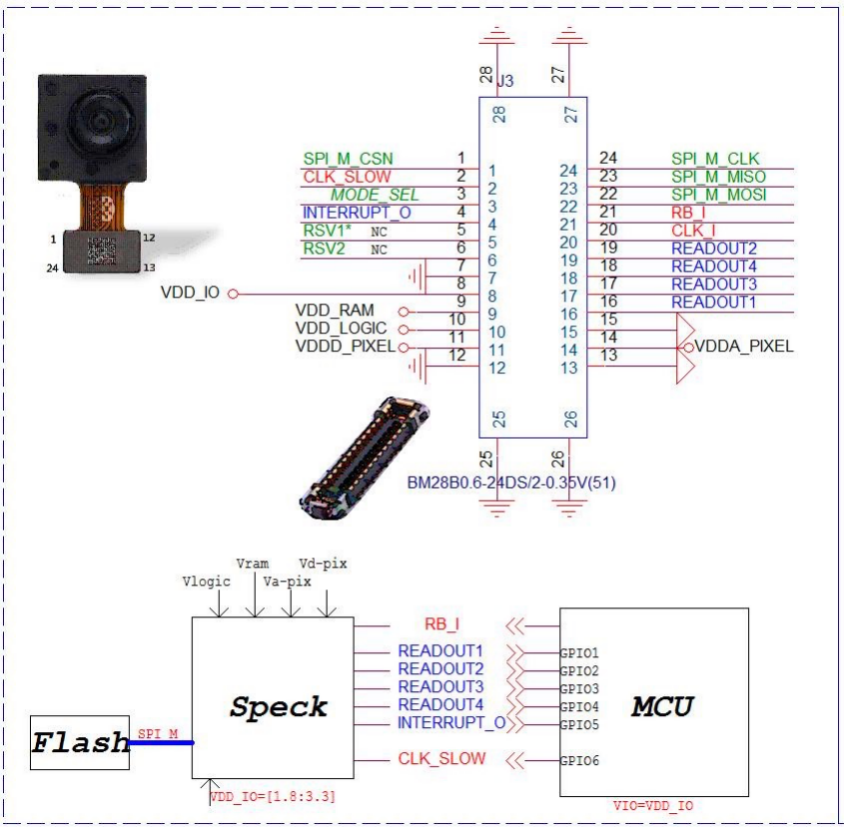



Figure 9 . Hardware connection 1

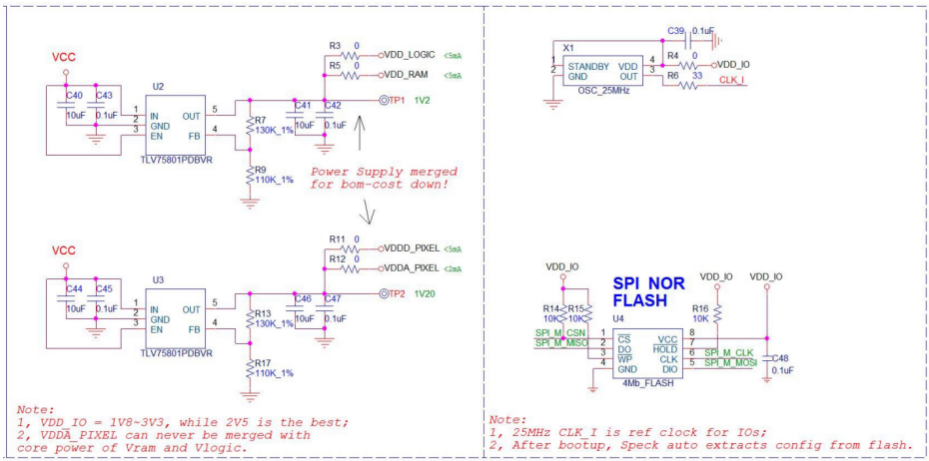



Figure 1 0 . Peripheral circuitry in hardware connection 1

## Note:

- Ensure that the values of the registers are set correctly in the configuration file so that pin16-19 on the module connector is used as READOUT [1:4];
- The 4 power rails for DVS and NPU (DynapTMCNN Processor core) are best supplied separately, or can be combined appropriately to save cost (refer to the figure above);
- SLOW_CLK is the reference time-window for the chip output (Interrupt_O + READOUT [1:4]), the frequency of which should be determined by the specific application and is generally less than 1k;
- Ultra-low-power chip SpeckTM output IO drive is very weak, need to do drive enhancement before direct drive peripherals such as LEDs.

## 5.2. Speck™ is activated and configuration is downloaded from the external processor

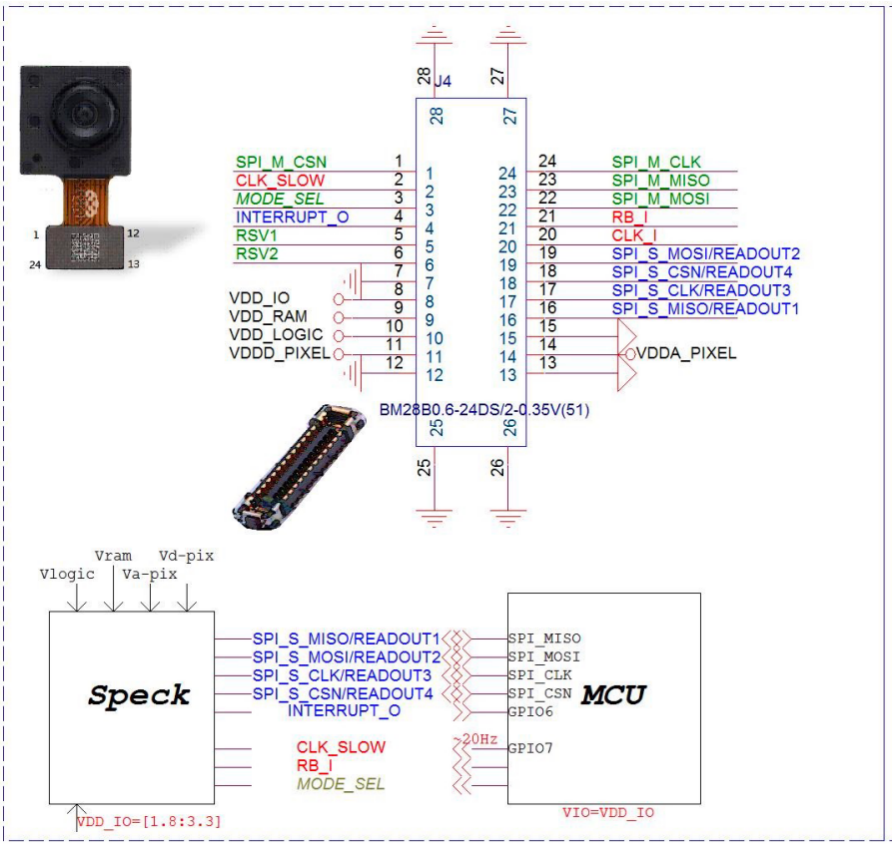



Figure 1 1. Hardware connection 2

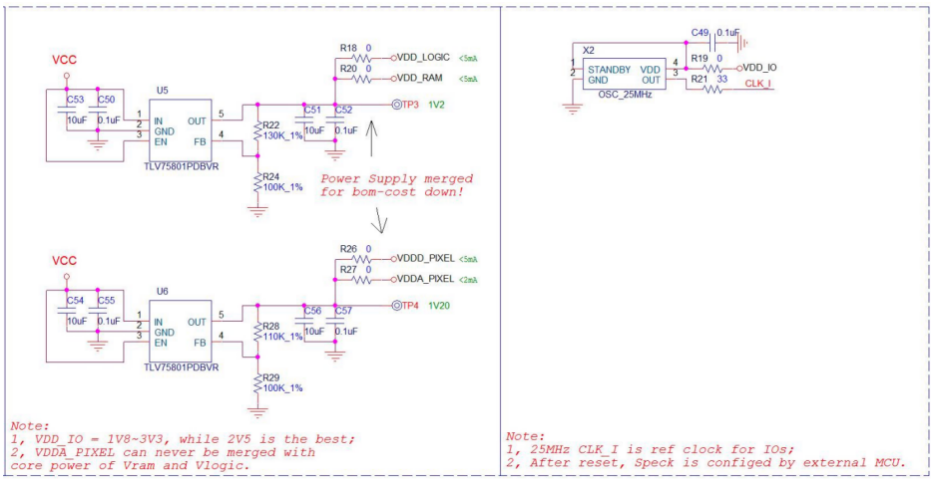



Figure 1 2 . Peripheral circuitry in hardware connection 2

## Note:

- When the SpeckTM chip is configured by the external processor, by default pins 16-19 on the module connector are used as SPI-slave (you should make sure that the internal registers are set to the correct values and that SPI_M_MISO is grounded);
- The 4 power rails for DVS and NPU (DynapTMCNN Processor core) are preferably supplied separately, or can be combined appropriately to save cost, refer to the above figure);
- After reset and power-on, the external processor configures the SpeckTM chip or accesses the on-chip registers/rams via SPI-slave (module pin16--19); after the configuration is complete, the internal registers can be set to multiplex the pin16--19 function of the module to READOUT [1:4] for the chip outputs; the settings of the registers take effect immediately; After reset or power failure, the configuration (configuration file and register values) is invalidated;
- SLOW_CLK is the reference time-window for the chip outputs (Interrupt_O + READOUT [1:4]), the frequency of which should be determined by the specific application and is generally less than 1k;

## 5.3. Output pin descriptions

- By default, the initial state of the output (Interrupt_O + READOUT [1:4]) pins of the SpeckTM chip/module are all low ("0"):
- When the value of (any one of) the maximum active class in an algorithmic task executed by the chip exceeds the preset threshold, or the preset threshold is manually modified (made smaller), then the Interrupt_O pin will be briefly set high (*) during the low cycle segment of SLOW_CLK; and Interrupt_O will be constantly low during the high cycle segment of SLOW_CLK;
- READOUT[1:4] reacts to the index number of the most active category in the output of the result of the algorithm executed by the chip: as soon as the peak value of an active category exceeds the preset threshold or the preset threshold is manually modified (made smaller) during the cycle of SLOW_CLK, the index number corresponding to that active category is activated and output (reacted to) to the READOUT[1:4] pins;
- The outputs of the SpeckTM chips/modules (Interrupt_O + READOUT [1:4]) are referenced to SLOW_CLK: where, during a SLOW_CLK "read out" cycle, the Interrupt_O pin is briefly (<3us) pulled high (set to "1") and then quickly updated back to a "low" state (set to "0"), while the READOUT [1:4] state is quickly updated back to a "low" state (set to "0"). "1") during a SLOW_CLK "read-out" cycle, then it is quickly updated back to the "low" state (set to "0"), and the READOUT [1:4] state remains for the length of a SLOW_CLK cycle length, and the state of READOUT [1:4] will remain for the length of one SLOW_CLK cycle until the next Interrupt_O state change (refer to Figure 12 below).


Figure 1 3 . (Interrupt_O + READOUT [1:4]), refer to SLOW_CLK

- As can be seen from the above figure, when the chip executes the algorithmic task and has a clear calculation result, there must be a flip of the output pin state; each READOUT [1:4] signal change must be accompanied by a change in the Interrupt_O signal, that is, the SpeckTM chip outputs a maximum of 16 different classification results; however, it should be noted that: the invalid classification must occupy one, that is, the algorithmic model is a maximum of 15 valid classifications can be obtained;

- The 4-bit READOUT output responds to the most recent sequence number of the most active category; thus, for example, in applications where only 4 categories are required, the CNN layer can be configured such that the 4 READOUT output category sequence numbers are encoded as 1, 2, 4, and 8, at which point each of the READOUT output pins corresponds to exactly one of the most interesting categories (sequences) directly, without the need for the decoder to do any further binary digit parsing;
- In particular, as a valid classification in the algorithmic model, if the hardware sets the output pin mapping to READOUT[1:4] = 0000, the hardware output result/waveform of the chip will have only the signal of the Interrupt_O pin appearing (transiently) high while the READOUT[1:4] pins remain "low" in the corresponding SLOW_CLK cycle; and the READOUT[1:4] pins remain "low"; and the Interrupt_O pin will be (briefly) high in the corresponding SLOW_CLK cycle; and the READOUT[1:4] pins remain "low". :4] pin remains "low";
- Therefore, when the SpeckTM configuration is complete and the computation is executed, the external processor can wake up the system to get the result of the computation contained in READOUT [1:4] by listening for a state change in Interrupt_O (refer to Chapter 7: Post-Processing).

**Note:** There is a very short delay between Interrupt and the falling edge of slow-clk, and between READOUT [1:4] and the rising edge of slow-clk.

## 5.4. SPI-slave interface description

The Speck™ chip supports an external processor to access and modify the values of on-chip registers and srams through the SPI-slave interface. This SPI-slave interface supports modes 0 and 3 with a maximum rate of CLK/16 (if CLK=100Mhz, then SPI-clk is up to 6.25Mhz; correspondingly, if CLK=25Mhz, then SPI-clk is up to 1.5625Mhz) (SPI samples on the rising edge of the clock and reads out on the falling edge).

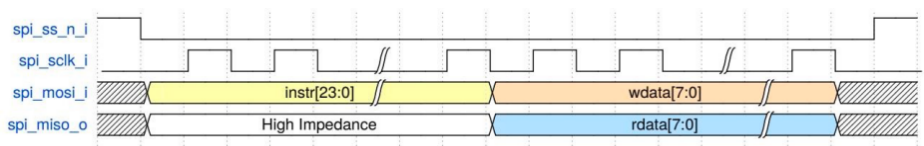



Figure 1 4 . SPI single access waveform schematic

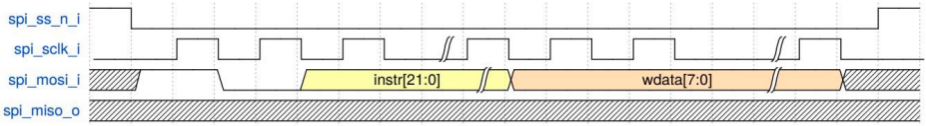



Figure 1 5. SPI single write waveform schematic

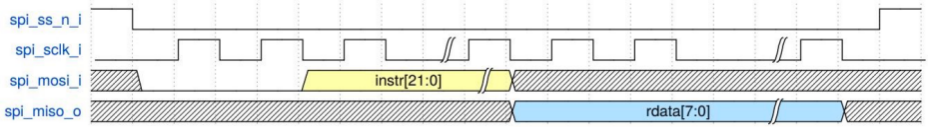



Figure 1 6. SPI single read waveform schematic

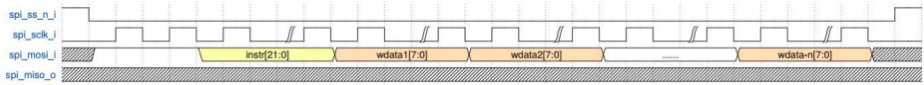



Figure 1 7. SPI burst write waveform schematic

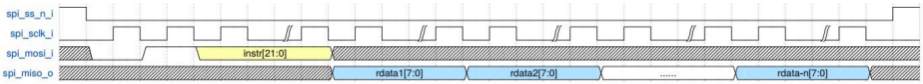



Figure 1 8. SPI burst read waveform schematic

# 6. Chip Configuration Approach

As mentioned above, there are two ways to configure the Speck™ chip: Speck™ actively grabs the configuration from an external flash via its own SPI (master) interface and Speck™ receives the configuration from an external processor via its own SPI (slave) interface. The configuration file contains the settings for the internal registers of the chip and the different CNN layers corresponding to the algorithmic models "written" to the on-chip sram (see Chapter 8.4, "Memory capacity").

## 6.1. Speck™ configuration bitstream generation with Samna

Here we demonstrate how to generate a default configuration in a Python environment:

```
import samna

# Getting the default configuration
config = samna.speck2f.configuration.SpeckConfiguration()

# Convert to binary
binary = samna.speck2f.configuration__to__flash_binary(cfg)

with open('config.bin', 'wb') as f:
    for b in binary:
        f.write((b).to_bytes( 1, byteorder = 'little'))
```

## 6.2. Speck™ automatically grabs configuration from flash

- Please follow the requirements specified by Samna and the correct register values should be set to ensure that modules pin16-19 can be used as chip outputs READOUT [1:4] to produce the bitstream correctly and write it to the appropriate type of FLASH chip using the burn-in basis;
- After the chip system is powered up and reset, given the correct interface reference clock (CLK_I), SpeckTM will prioritize the scanning of its SPI-master interface, sniffing whether there is an external flash device and the correct configuration file; if so, SpeckTM will automatically grab the configuration information from the flash;
- (If SPI-M-MISO is constantly low, or after a chip system scan timeout, SpeckTM switches to sniffing the SPI-slave interface, i.e., waiting for the external processor to download the configuration information.)

## 6.3. Configuration of Speck™ by external processor

The chip supports the passive configuration method (the external processor downloads the configuration file to Speck™ through the SPI-slave interface). When the chip is powered on, if the flash device and configuration file described in section 6.2 are not detected on the SPI-master interface, the chip can be configured by the external processor through the SPI-slave interface described in section 7.4.

**Configuration process:**

- The algorithm model completed on the devkit is used as the Speck chip configuration file (xxx.bin) by producing and exporting the bitstream file through the SynSense toolchain Samna; (Note: xxx is a customized filename here, same below);
- Use a small tool (config_gen.exe) on your PC to convert the configuration file into an array file (speck_config.c) recognizable by the MCU: Speck_config.c can be generated by typing config_gen.exe xxx.bin in cmd;
- Based on the reference clock CLK_I (frequency range 16MHz-50MHz, the higher the CLK_I, the shorter the configuration writing time of Speck algorithm model; however, the maximum rate of SPI interface writing configuration ≤ 1/16 CLK_I), the external processor writes the SpeckTM configuration in ROM to the SpeckTM chip via SPI interface;

**External processor resource requirements:**

- SPI master interface : 4-wire SPI (CSn,SCLK,MOSI,MISO), support mode 0 or mode 3;
- ROM : 354KiB to store the configuration (some MCUs support file compression to shrink the Speck™ configuration file to less than 50kiB);
- RAM : Depends on processor hardware specification and SPI driver;

# 7. Post Processing

Speck™ works always-on in real-world scenarios, i.e., it constantly analyzes and computes, and gives an sCNN-based classification index [0,1,2,3...15] in real-time (Speck™ supports a maximum of 15 valid classifications + 1 invalid classification). This index is represented by 4 Readout pin pins. The process of converting the 4-bit binary to a [0-15] classification index usually relies on external computational resources, e.g..

0011 → 3
1000→ 8
0101 → 5

In addition, external computational resources can further utilize the classification indexes to implement the intended logic operations/state machine transitions/frequency control/filtering, etc. For example:

- To minimize the occasional false positive output of the classifier: a counter can be used to count the number of consecutive occurrences of the same classification to match the threshold.
- In order to realize the state machine control of the switches: the state transitions in the state machine can be controlled using global variables on the MCU side using the outputs of the corresponding classifications.

**Note:** The approach to post-processing will vary for different application scenarios. More generally, post-processing refers to arithmetic/logic operations performed on Speck™ chip outputs using external resources (e.g., microprocessor), whose primary use is to calculate the sliding mean of up to 15 neurons within a reference time window, to provide a maximum mean of 15 neurons, and to compare the calculated sliding mean with a specified threshold.5 of Speck™ output pins ( Interrupt_O and READOUT[1:4]) are dedicated to the direct readout of the maximum activity level, and these pins are designed for the direct readout of the maximum peak category (with or without an activity threshold).

# 8. Appendix

## 8.1. Declaration of non-Ideal scenarios and influencing factors

The Speck™ chip integrates a Dynamic Vision Sensor (DVS) and a dedicated neuromorphic vision processing core (DYNAP™CNN) on-chip. The input of the entire chip system is light, and the illumination conditions directly and greatly affect, interfere with, or even damage the device's operating status. The main external factors are illuminance and flicker. In addition, like many other sensors, especially RGB sensors, dirt on the lens, smoke, fog, or direct obstruction in the scene can also affect or disrupt the normal execution of the system's application. Furthermore, extreme (high or low) temperatures can also affect or even damage the normal operation of the silicon-based chip.

### 8.1.1 Illumination

All sensors produce both signals and noise at the same time. For light-dependent sensors such as Dynamic Vision Sensors (DVS), the signal (valid event) is greatly reduced under low illumination, and the background noise increases. While the target action contour may be vaguely visible to the naked eye, it presents a significant challenge for algorithm models. In fact, all major DVS manufacturers currently have a very wide dynamic range for on-chip Dynamic Vision Sensors (DVS) measured in the laboratory, theoretically supporting imaging at very low illumination levels. However, in this case, the effective "events" are too sparse to effectively support application requirements.

The dynamic vision sensor (DVS) integrated in the Speck™ chip by SynSense Technology is capable of supporting imaging under lighting conditions as low as 10 lux, according to data obtained in the laboratory. However, in typical application scenarios, it has been found:

- In a 10~20 lux environment, the current application algorithm model performance shows a significant decrease.
- In scenes with 20-50 lux lighting conditions, there is a slight increase in delay in the application algorithm model, which may result in missed or erroneous judgments (<5%);
- In scenes with lighting conditions greater than 50 lux, the application algorithm model works stably and produces highly reliable results (>95%);

China National Illumination Standards (excerpted).

| Residential Building Lighting Standards | | |
|---|---|---|
| **Room or Area** | **Reference Plane and Height** | **Illumination Standards (lx)** |
| Living Room (General Activity) | 0.75m Horizontal Plane | 100 |
| Living Room (Writing, Reading) | 0.75m Horizontal Plane | 300 |
| Bedroom (General Activity) | 0.75m Horizontal Plane | 75 |
| Bedroom (Writing, Reading) | 0.75m Horizontal Plane | 150 |
| Dining Room | 0.75m Table Surface | 150 |
| Kitchen (General Activity) | 0.75m Horizontal Plane | 100 |
| Kitchen (Operation Table) | Table Surface | 150 |
| Bathroom | 0.75m Horizontal Plane | 100 |
| **Note**: Mixed lighting is recommended. | | |

| Commercial Building Lighting Standards | | |
|---|---|---|
| **Room or Area** | **Reference Plane and Height** | **Illumination Standards (lx)** |
| General Store | 0.75m Horizontal Plane | 300 |
| High-End Store | 0.75m Horizontal Plane | 500 |
| General Supermarket | 0.75m Horizontal Plane | 300 |
| High-End Supermarket | 0.75m Horizontal Plane | 500 |
| Cashier Desk | Table Surface | 500 |

| Library Building Lighting Standards | | |
|---|---|---|
| **Room or Area** | **Reference Plane and Height** | **Illumination Standards (lx)** |
| General Reading Room | 0.75m Horizontal Plane | 300 |
| National, Provincial and Other Important Libraries' Reading Room | 0.75m Horizontal Plane | 500 |
| Elderly Reading Room | 0.75m Table Surface | 500 |
| Rare Books and Documents Reading Room | 0.75m Horizontal Plane | 500 |
| Exhibition Hall, Catalog Hall, Cashier's Hall | 0.75m Horizontal Plane | 300 |
| Bookstacks | 0.25m Horizontal Plane | 50 |
| Workspace | 0.75m Horizontal Plane | 300 |

| Office Building Lighting Standards | | |
|---|---|---|
| **Room or Area** | **Reference Plane and Height** | **Illumination Standards (lx)** |
| General Office | 0.75m Horizontal Plane | 300 |
| High-Grade Office | 0.75m Horizontal Plane | 500 |
| Conference Room | 0.75m Table Surface | 300 |
| Reception Desk, Front Desk | 0.75m Horizontal Plane | 300 |
| Sales Hall | 0.75m Horizontal Plane | 300 |
| Design Room | Actual Work Surface | 500 |
| Document Organization, Copying and Distribution Room | 0.75m Horizontal Plane | 300 |
| Data Archive Room | 0.75m Horizontal Plane | 200 |

| Lighting Standards for School Buildings | | |
|---|---|---|
| **Room or Area** | **Reference Plane and Height** | **Illumination Standards (lx)** |
| Classroom | Desk surface | 300 |
| Laboratory | Laboratory table surface | 300 |
| Art room | Table surface | 500 |
| Multimedia classroom | 0.75m above horizontal plane | 300 |
| Classroom blackboard | Blackboard surface | 500 |

| Lighting Standards for Hospital Buildings | | |
|---|---|---|
| **Room or Area** | **Reference Plane and Height** | **Illumination Standards (lx)** |
| Treatment room | 0.75m above horizontal plane | 300 |
| Laboratory | 0.75m above horizontal plane | 500 |
| Operating room | 0.75m above horizontal plane | 750 |
| Consulting room | 0.75m above horizontal plane | 300 |
| Waiting room, registration hall | 0.75m above horizontal plane | 200 |
| Ward | Floor surface | 100 |
| Nurse station | 0.75m above horizontal plane | 300 |
| Pharmacy | 0.75m above horizontal plane | 500 |
| Intensive care unit | 0.75m above horizontal plane | 300 |

| Lighting Standards for Public Places | | |
|---|---|---|
| **Room or Area** | **Reference Plane and Height** | **Illumination Standards (lx)** |
| Lobby (ordinary) | Floor surface | 100 |
| Lobby (luxury) | Floor surface | 200 |
| Corridors and passageways (ordinary) | Floor surface | 50 |
| Corridors and passageways (luxury) | Floor surface | 100 |
| Stairs and platforms (ordinary) | Floor surface | 30 |
| Stairs and platforms (luxury) | Floor surface | 75 |
| Escalators | Floor surface | 150 |
| Toilets, bathrooms (ordinary) | Floor surface | 75 |
| Toilets, bathrooms (luxury) | Floor surface | 150 |
| Elevator lobby (ordinary) | Floor surface | 75 |
| Elevator lobby (luxury) | Floor surface | 150 |
| Rest room | Floor surface | 100 |
| Storage room, warehouse | Floor surface | 100 |
| Garage (ordinary) | Floor surface | 75 |
| Garage (luxury) | Floor surface | 200 |
| **Note**: The lighting standards for power stations and substations in residential and public buildings shall be selected from the table. | | |

### 8.1.2 Flicker

- Like all light-based sensors, the Dynamic Vision Sensor (DVS) integrated within the Speck™ chip is also sensitive to low-frequency "on/off" flickers of light. From the imaging principle of the DVS, for low-frequency flickers, effective "events" can be

easily overwhelmed by flicker noise.

- The Speck™ chip can operate normally under the power frequency flicker conditions that comply with the GB/T31831 "LED Indoor Lighting Technology Application Requirements" national standard. For power frequency flicker exceeding the national standard, the integrated anti-flicker filter in the Speck™ chip can be enabled to optimize the on-chip power frequency filter. However, due to the complex types of power frequency flicker scenarios that exceed the national standard, the built-in anti-flicker filter cannot completely eliminate/effectively suppress all non-national standard flickers.
- In practical applications, as long as the main light source does not have flicker frequency bands or flicker depth beyond the national standard, ambient light will not cause significant interference or damage to the application model of Speck™. In other words, Speck™ and the application algorithm model itself can tolerate some minor flickers (flicker frequency and depth of direct and reflected light from the target) of secondary light sources in the application scenario that exceed the national standard (low-risk area, see Chapter 8.2).

### 8.1.3 Obstruction, smoke and fog

- Obstruction can affect the integrity of imaging and directly damage the correct execution of algorithmic models.
- Mild smoke and fog can be tolerated by the applied algorithmic model, but dense smoke or fog is like the lens being obstructed.

### 8.1.4 Extreme temperatures

- The dynamic visual sensor (DVS) integrated on the Speck™ chip contains a large number of analog circuits that are temperature-sensitive. If the temperature exceeds the application scenarios supported by the manufacturer, it will directly lead to partial loss of the imaging function of the DVS, and in severe cases, it will directly fail.
- The production of the Speck™ optical module is similar to that of the RGB optical module. Considering the production process of the module, it is also not suitable for use under temperature conditions beyond the support range. Currently, the Speck™ chip and optical module can be used in an environment of 0-65°C, and it is strongly recommended to use it in a scene of 15-65°C to ensure more stable DVS imaging.

## 8.2. Non-standard flicker

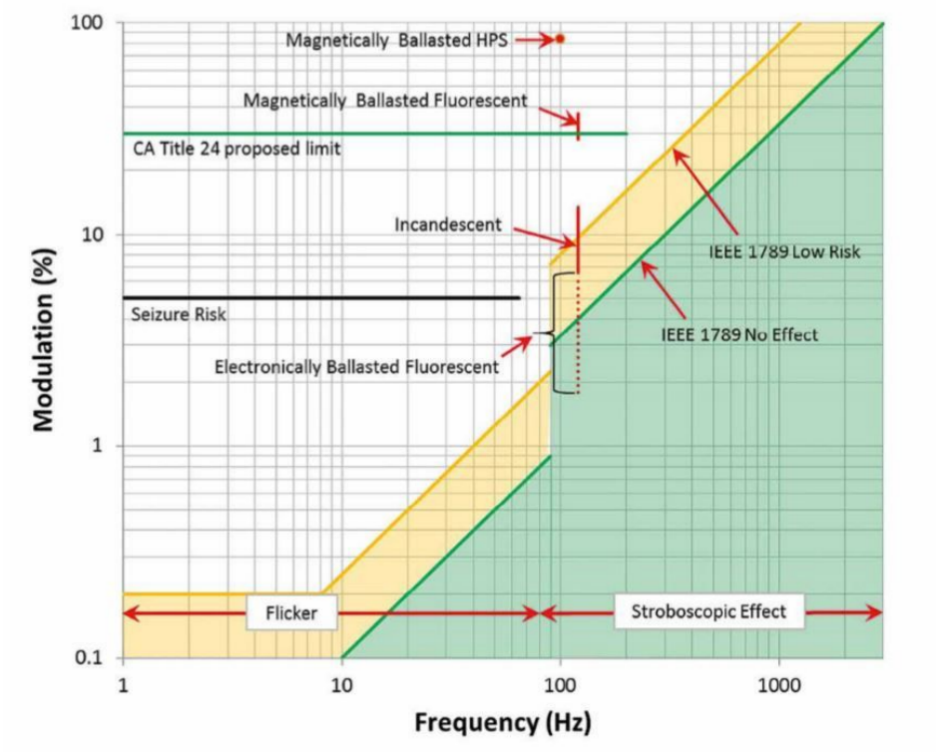



Figure 1 9 . IEEE 1789 'Recommended Practices' for Light Flicker

According to the IEEE std 1789-2015 document, the luminaire strobe low risk limits can be referred to the following table:

| Flicker Percentage (Flicker Depth) Requirements for Low-Risk | |
|---|---|
| **Flicker (Modulation) Frequency f** | **Flicker Percentage (FPF) Limitation Value %** |
| <8Hz | FPF≦0.2 |
| 8 - 90HZ | FPF≦0.025 × f |
| 90 - 1250Hz | FPF≦0.08 × f |
| >1250Hz | Low-risk exemption |

According to the domestic GB/T31831 document "Application Requirements for LED Indoor Lighting Technology", the harmless limit of flicker percentage for lamps is specified in the table below:

| Flicker Percentage (Flicker Depth) Requirements for Harmless | |
|---|---|
| **Flicker (Modulation) Frequency f** | **Flicker Percentage (FPF) Limitation Value %** |
| 10 - 90HZ | FPF ≦0.01 × f |
| 90 - 3125Hz | FPF ≦0.08 × f / 2.5 |
| f >3125Hz | High-frequency exemption |

## 8.3. Measured power consumption in a typical application scenario

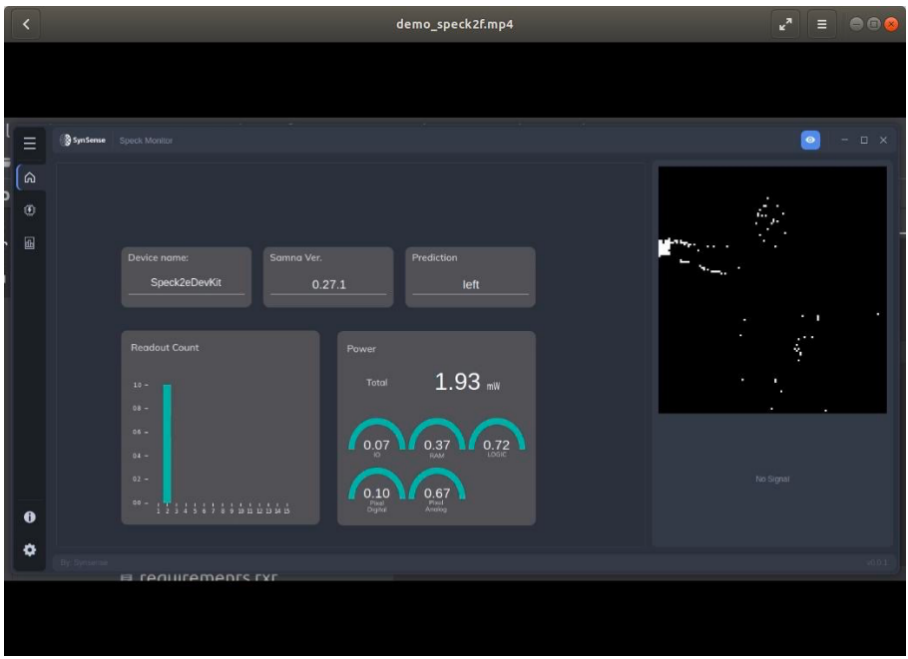



Figure 2 0 . A body gesture model uses 4 layers of CNN resources (IO=2V5, other power rails are 1V2)

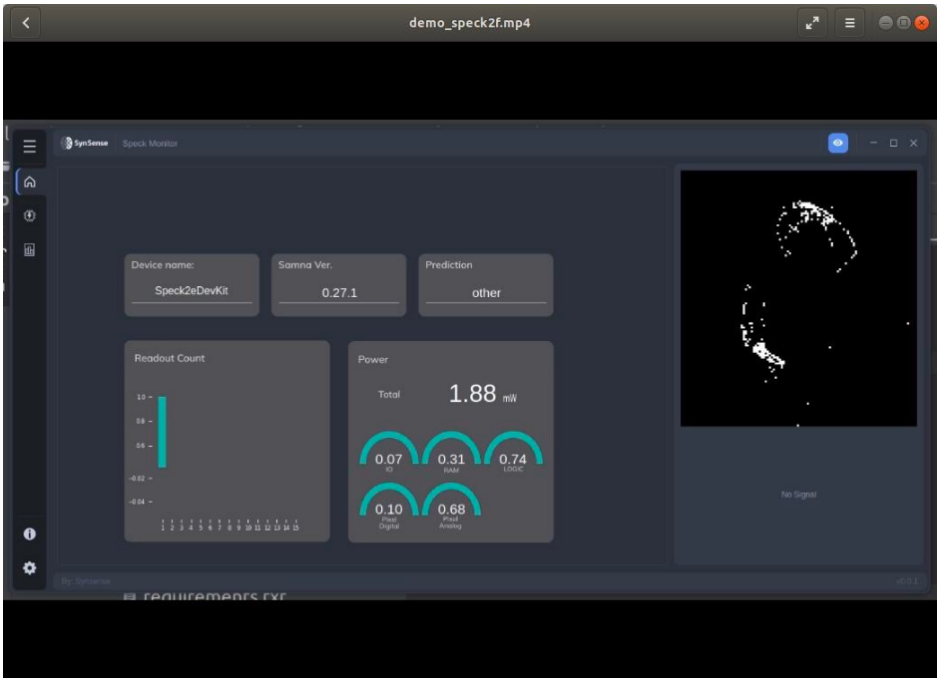



Figure 2 1. A body gesture model uses 4 layers of CNN resources (IO=2V5, other power rails are 1V2)

**Note:** Screenshot from Samna visualizer.

## 8.4. Memory capacity

The Speck™ is divided into 9 cores, each of which executes a single CNN layer. The memory capacities of the cores are different, and restrict the implementation of larger layers to specific cores.

| Core. | Kernel memory (WORD) | Leak memory (WORD) | Neuron memory (WORD) |
|---|---|---|---|
| 0 | 16 Ki | 1 Ki | 64 Ki |
| 1 | 16 Ki | 1 Ki | 64 Ki |
| 2 | 16 Ki | 1 Ki | 64 Ki |
| 3 | 32 Ki | 1 Ki | 32 Ki |
| 4 | 32 Ki | 1 Ki | 32 Ki |
| 5 | 64 Ki | 1 Ki | 16 Ki |
| 6 | 64 Ki | 1 Ki | 16 Ki |
| 7 | 16 Ki | 1 Ki | 16 Ki |
| 8 | 16 Ki | 1 Ki | 16 Ki |

| SRAM | Filter memory (WORD) |
|---|---|
| DVS Filter | 16 Ki |

| | Memory Type | Word Length |
|---|---|---|
| 1 | Kernel | 8 bits |
| 2 | Neuron | 16 bits |
| 3 | Leak | 16 bits |
| 4 | Filter | 16 bits |

Let a network be defined by the number of input features c, the number of output features f, and the kernel dimensions $k_x$ and $k_y$.

The theoretical number of WORDs required for kernel memory $K_M$ is then

$$K_M = cf\, k_x\, k_y$$

The total number of memory WORDs required is

$$K_{MT} = c \cdot 2^{\lceil \log_2 (k_x k_y) \rceil + \lceil \log_2 (f) \rceil}$$

The required number of neuron memory WORDs NM depends on the dimensions of the input features $c_x$ and $c_y$, as well as the stride and padding $s_x$, $s_y$, and $p_x$, $p_y$.

$$f_x = \frac{c_x - k_x + 2p_x}{S_x} + 1$$

$$f_y = \frac{c_y - k_y + 2p_y}{S_y} + 1$$

$$N_M = f\, f_x\, f_y$$

Again the total number of required WORDs on the chip side is larger.

$$N_{MT} = f \cdot 2^{\lceil \log_2 (f_y) \rceil + \lceil \log_2 (f_x) \rceil}$$

## 8.5. 1.98mm optical module specification

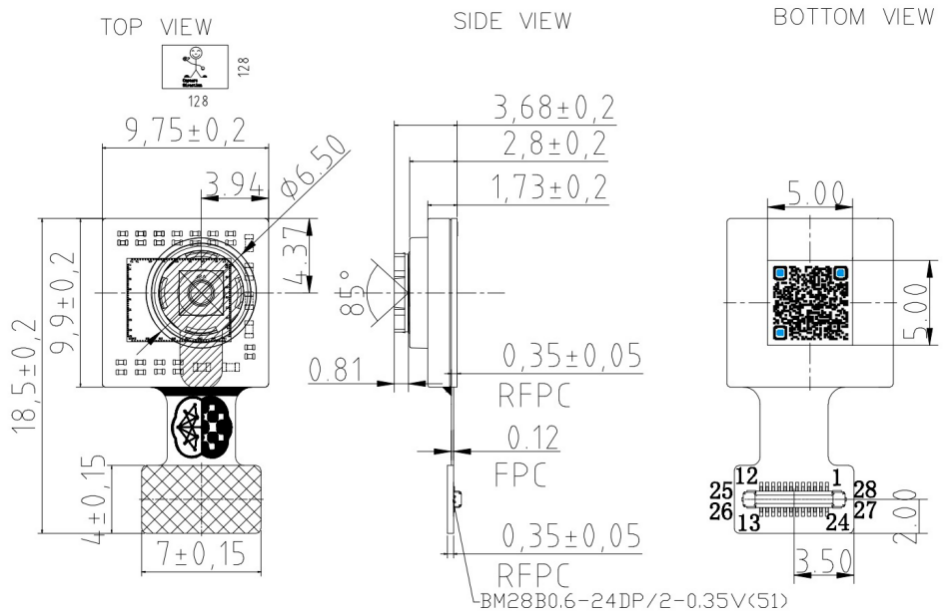



Figure 2 2. Size of the 1.98mm lens

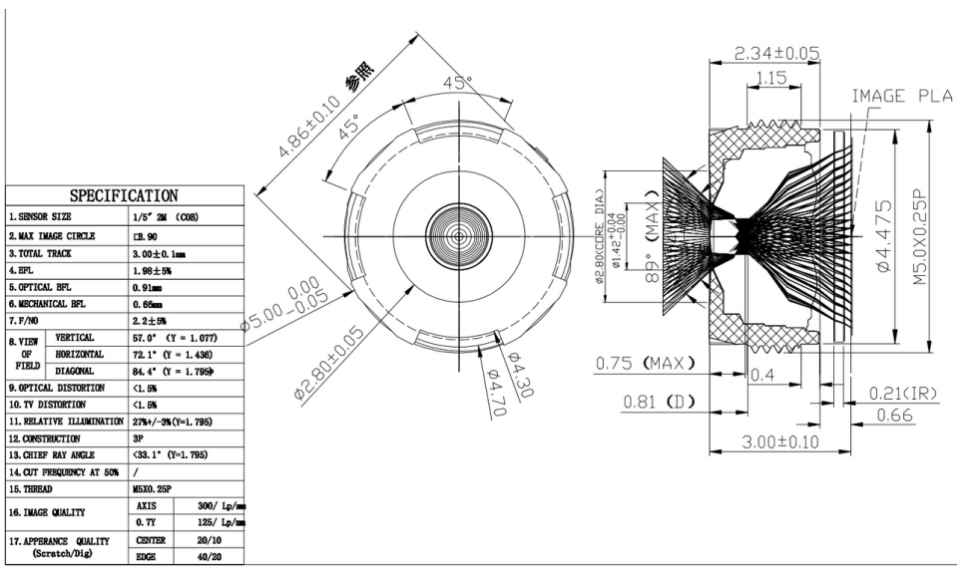



Figure 2 3. Specification of the 1.98mm lens

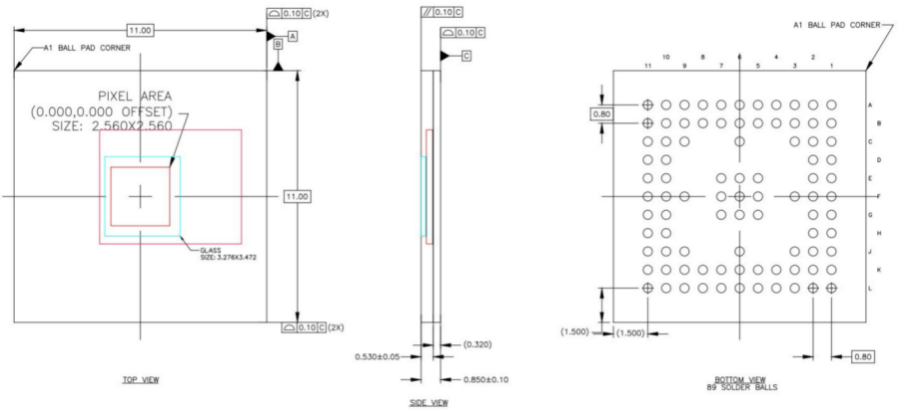
According to the formula:

HFOV = 2 * ARCTAN(H / (2 * EFL)), VFOV = 2 * ARCTAN(V / (2 * EFL)),

The H-FOV=65.8°，V-FOV=65.8°（where H = V = 2.56mm）for 1.98mm lens.

## 8.6. LGA engineering sample

### 8.6.1 Package diagram




### 8.6.2 Pin out

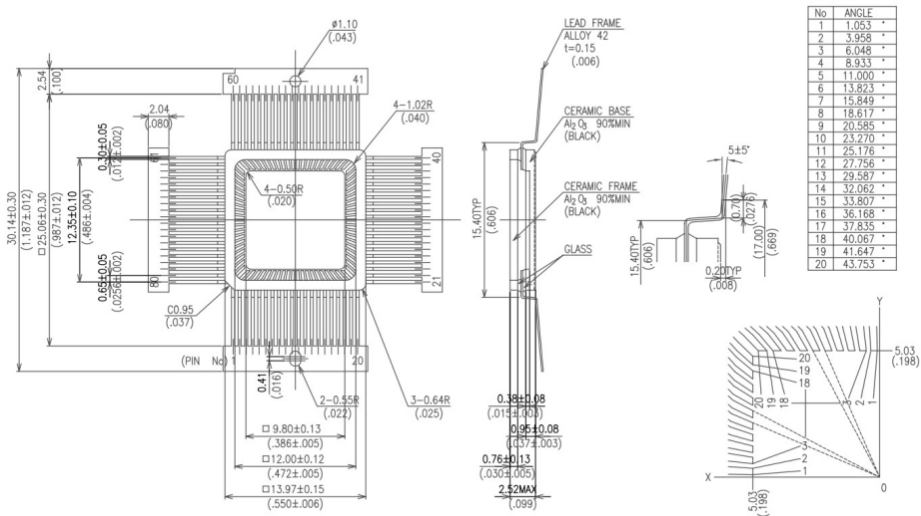
| Pin Number | Net Name |
|---|---|
| A1 | PAD_IO20_READOUT1_O |
| A2 | VSSD |
| A3 | PAD_IO27_P2S_OUT2_O |
| A4 | PAD_IO18_P2S_OUT1_O |
| A5 | PAD_IO19_P2S_DREADY_O |
| A6 | PAD_IO1_CLK_I |
| A7 | PAD_IO2_RB_I |
| A8 | PAD_IO16_S2P_DATA_I |
| A9 | PAD_IO15_S2P_DREADY_I |
| A10 | PAD_GPIO13_SPI_S_CLK_IO |
| A11 | PAD_IO17_S2P_CREADY_O |
| B1 | PAD_IO21_READOUT2_O |
| B2 | VSSD |
| B3 | VDDIO |
| B4 | VSSD |
| B5 | VSSD |

| | |
|---|---|
| B6 | VSSD |
| B7 | VDDIO |
| B8 | VDD_RAM |
| B9 | VDDIO |
| B10 | |
| B11 | PAD_GPIO11_SPI_S_MISO_O |
| C1 | PAD_IO25_CLK_SLOW_I |
| C2 | VDDIO |
| C3 | VSSD |
| C6 | VSSD |
| C9 | VSSD |
| C10 | VP |
| C11 | PAD_GPIO12_SPI_S_MOSI_IO |
| D1 | PAD_IO22_READOUT3_O |
| D2 | VDD_RAM |
| D10 | |
| D11 | PAD_GPIO14_SPI_S_SS_N_IO |
| E1 | VSSD |
| E2 | VSSD |
| E5 | VSSD |
| E6 | VSSD |
| E7 | VSSD |
| E10 | VSSD |
| E11 | PAD_GPIO10_SPI_M_SS_N_IO |
| F1 | VSSD |
| F2 | VP |
| F3 | VSSD |
| F5 | VSSD |
| F6 | VSSD |
| F7 | VSSD |
| F9 | VP |
| F10 | VDDIO |
| F11 | PAD_GPIO9_SPI_M_CLK_IO |
| G1 | VSSD |
| G2 | VSSD |
| G5 | VSSD |
| G6 | VSSD |
| G7 | VSSD |
| G10 | VDDIO |
| G11 | PAD_GPIO8_SPI_M_MOSI_IO |

| | |
|---|---|
| H1 | VDDD_PIXEL |
| H2 | VSSD |
| H10 | VP |
| H11 | PAD_GPIO7_SPI_M_MISO_IO |
| J1 | VDDD_PIXEL |
| J2 | VSSD |
| J3 | VDDIO |
| J6 | VDDIO |
| J9 | VDD_RAM |
| J10 | VSSD |
| J11 | VSSD |
| K1 | PAD_IO26_MODE_SEL_I |
| K2 | VSSD |
| K3 | VSSD |
| K4 | VDDIO |
| K5 | VP |
| K6 | VP |
| K7 | VSSD |
| K8 | VSSD |
| K9 | VSSD |
| K10 | VSSD |
| K11 | VDDIO |
| L1 | PAD_IO23_READOUT4_O |
| L2 | VDDA_PIXEL |
| L3 | VDDA_PIXEL |
| L4 | VSSA |
| L5 | VSSA |
| L6 | VREF |
| L7 | PAD_IO24_INTERRUPT_O |
| L8 | PAD_IO6_TDO_O |
| L9 | PAD_IO5_TMS_I |
| L10 | PAD_IO4_TDI_I |
| L11 | PAD_IO3_TCK_I |

## 8.7. QFP80 engineering sample

### 8.7.1 Package diagram




| No | ANGLE |
|---|---|
| 1 | 1.053 ° |
| 2 | 3.958 ° |
| 3 | 6.048 ° |
| 4 | 8.933 ° |
| 5 | 11.000 ° |
| 6 | 13.823 ° |
| 7 | 15.849 ° |
| 8 | 18.617 ° |
| 9 | 20.585 ° |
| 10 | 23.270 ° |
| 11 | 25.176 ° |
| 12 | 27.756 ° |
| 13 | 29.587 ° |
| 14 | 32.062 ° |
| 15 | 33.807 ° |
| 16 | 36.168 ° |
| 17 | 37.835 ° |
| 18 | 40.067 ° |
| 19 | 41.647 ° |
| 20 | 43.753 ° |

### 8.7.2 Pin out

| Pin No. | Pad Name |
|---|---|
| 1 | VDDIO |
| 2 | PAD_IO40_RGB_PCLK_I |
| 3 | PAD_IO20_READOUT1_O |
| 4 | PAD_IO29_RGB_HREF_I |
| 5 | VP |
| 6 | vdd_ram |
| 7 | PAD_IO21_READOUT2_O |
| 8 | PAD_IO25_CLK_SLOW_I |
| 9 | PAD_IO22_READOUT3_O |
| 10 | VDDIO |
| 11 | VP |
| 12 | VBIAS |
| 13 | PAD_IO28_RGB_VSYNC_I |
| 14 | vssd_pixel |
| 15 | vddd_pixel |
| 16 | vssa_pixel |
| 17 | vdda_pixel |
| 18 | PAD_IO31_RGB_INT_CLK_I |
| 19 | PAD_IO26_MODE_SEL_I |
| 20 | VDDIO |

| | |
|---|---|
| 21 | PAD_IO32_RGB_D2_I |
| 22 | PAD_IO23_READOUT4_O |
| 23 | vdda_pixel |
| 24 | vssa_pixel |
| 25 | PAD_IO33_RGB_D3_I |
| 26 | VREF |
| 27 | VP |
| 28 | VDDIO |
| 29 | PAD_IO24_INTERRUPT_O |
| 30 | PAD_IO34_RGB_D4_I |
| 31 | PAD_IO6_TDO_O |
| 32 | vdd_ram |
| 33 | vss_ram |
| 34 | VP |
| 35 | VG |
| 36 | PAD_IO5_TMS_I |
| 37 | PAD_IO4_TDI_I |
| 38 | PAD_IO3_TCK_I |
| 39 | VDDIO |
| 40 | PAD_GPIO7_SPI_M_MISO_IO |
| 41 | PAD_IO36_RGB_D6_I |
| 42 | PAD_GPIO8_SPI_M_MOSI_IO |
| 43 | VDDIO |
| 44 | VSSIO |
| 45 | PAD_IO37_RGB_D7_I |
| 46 | PAD_GPIO9_SPI_M_CLK_IO |
| 47 | VDDIO |
| 48 | PAD_IO38_RGB_D8_I |
| 49 | PAD_GPIO10_SPI_M_SS_N_IO |
| 50 | PAD_IO39_RGB_D9_I |
| 51 | VP |
| 52 | PAD_GPIO14_SPI_S_SS_N_IO |
| 53 | PAD_GPIO11_SPI_S_MISO_O |
| 54 | PAD_GPIO12_SPI_S_MOSI_IO |
| 55 | PAD_IO17_S2P_CREADY_O |
| 56 | PAD_GPIO13_SPI_S_CLK_IO |
| 57 | PAD_IO15_S2P_DREADY_I |
| 58 | PAD_IO16_S2P_DATA_I |
| 59 | PAD_IO2_RB_I |
| 60 | vdd_ram |
| 61 | PAD_IO1_CLK_I |
| 62 | PAD_IO19_P2S_DREADY_O |
| 63 | PAD_IO18_P2S_OUT1_O |
| 64 | PAD_IO27_P2S_OUT2_O |

## 8.8. Others

For a more detailed explanation of the reading principle and method for the Speck™ chip output, as well as instructions for configuring and utilizing the on-chip CNN and other resources, please contact technical support or visit SynSense's publicly available materials on GITLAB.

# 9. Change Log

| No. | Ver | Date | Editor | Changes |
|---|---|---|---|---|
| 1 | V0.1 | 2023.02 | FAE | Initial version |
| 2 | V0.2 | 2023.03 | FAE | Update 8.1.2 and 8.4 |
| 3 | V0.3 | 2023.07 | FAE | Added 8.5 |
| 4 | V0.4 | 2025.02 | Billy | Added 8.6 and 8.7 |

# Make Intelligence Smarter

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