Xylo™ Audio
Customer Datasheet
Aug 2023

The information contained herein is for informational purposes only, and is subject to change without notice.

Intellectual Property Rights

SynSense owns the copyrights, trademarks and other intellectual property rights and interests in this document. The fact that SynSense provides this document to you does not affect the rights and interests of SynSense as described above.

Brand and product names are trademarks or registered trademarks of their respective owners.

No license, including implied or arising by estoppel, to any intellectual property rights is granted by this document.

No Warranty

While every precaution has been taken in the preparation of this document, it may contain technical inaccuracies, omissions and typographical errors, and SynSense is under no obligation to update or otherwise correct this information. SynSense makes no representations or warranties with respect to the accuracy or completeness of the contents of this document, and assumes no liability of any kind, including the implied warranties of noninfringement, merchantability or fitness for particular purposes, with respect to the operation or use of SynSense hardware, software or other products described herein.

Disclaimer

To the extent permitted by applicable law, SenSense shall not be liable for any direct, indirect, incidental, special, incidental or other damages, costs, liabilities or claims of any kind arising out of or in connection with the use of this document,with respect to the operation or use of SynSense hardware, software or other products described herein.

Applicable Terms and Conditions for Products

Terms and limitations applicable to the purchase or use of SynSense's products are as set forth in a signed agreement between you and SynSense or in SynSense's Standard Terms and Conditions.

Xylo^{TM}Audio 3 Customer Datasheet

Xylo^{TM}Audio 3 is an ultra-low-power always-on mixed signal AI chip for auditory processing, based on 3rd generation Artificial Neural Network, i.e., Spiking Neural Network (SNN).

With proper network design and training Xylo^{TM}Audio 3 could support various battery-powered auditory applications, for example:

- Key word spotting (KWS)
- Vibration anomaly detection, e.g. machine abnormal status detection in factory
- Ambient sound detection, e.g. baby crying in noisy environment
- Mobile / wearable devices control
- Voice activated intelligent personal assistants
- Agricultural monitoring to detect pests or precipitation
- Security / safety monitoring to identify intruders or dangerous conditions.
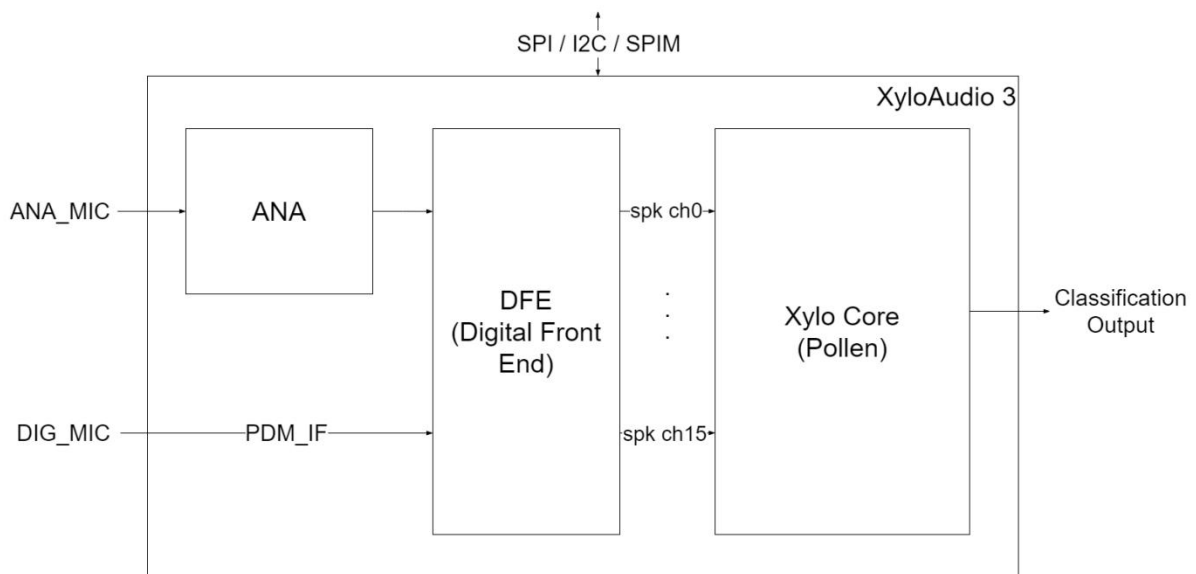
1.   Block diagram

Figure 1 . Xylo^{TM}Audio 3 block diagram

2. Key features

- Supports analog microphone (ANA_MIC)
  - Fully differential analog microphone input that supports 50Hz - 20kHz audio signal with a common mode voltage from 0V to 1.1V
- Supports digital microphone (DIG_MIC) via 2-wire PDM IF (PDM_CLK and PDM_DATA)
  - PDM_CLK up to 1.5 MHz, input or output direction
  - mono channel, PDM_DATA sampled at rising or falling edge of PDM_CLK
- Supports 2-wire I2C slave IF (up to Fast-mode Plus, 1 MHz), 4-wire SPI slave IF (up to 3.125 MHz, both single and burst mode) and 4-wire SPI master IF (up to 50 MHz)
- Supports up to 992 hidden neurons (HN) and up to 32 classifications
- Supports both Direct Output Mode (DOM) and Interrupt Mode (IM) for classification result
- Up to 50 MHz internal operating frequency
- Extremely low memory footprint (~124 KB), memory power control granularity down to 2 KB
- Ultra-low average working power consumption (<300 µW)
- DFT logic included
- 4 mm x 4 mm QFN-32 package

3.   Electrical characteristics

Feature	Spec.	Units
Core Supply Voltage	1.1	V
IO Supply Voltage	2.5 / 3.3	V
Operating Temperature	0 ~ 70	℃
Digital Input High Voltage (VIH)	TBA / 2.0	V
Digital Input Low Voltage (VIL)	TBA / 0.8	V
Digital Output High Voltage (VOH)	TBA / 2.4	V
Digital Output Low Voltage (VOL)	TBA / 0.4	V
ANA_MIC Input Common Mode Voltage	0 ~ 1.1	V
Input Signal Frequency	50 ~ 20K	Hz
Audio Sampling Rate	50, 100, 200	KHz
Clock Frequency	50	MHz
Power Consumption	< 300	µW

4.   PIN location overview

Figure 2 . Xylo^{TM}Audio 3 PIN location overview

5. PIN list

#	Pin	Description
1	VDDQ	OTP Program Power Supply
2	ITEST	Analog Current Test
3	VTEST0	Analog Voltage Test 0
4	VINN	ANA_MIC input (negative)
5	VINP	ANA_MIC input (positive)
6	VTEST1	Analog Voltage Test 1
7	VSSIO	IO Ground
8	VDDIO	IO Power Supply
9	VSSA	Analog Ground
10	IFRC	Analog Test
11	VDDH	LDO Analog Power Supply
12	VDDHD	LDO Digital Power Supply
13	VDD	Core Power Supply
14	VSS	Core Ground
15	VSSIO	IO Ground
16	VDDIO	IO Power Supply
17	OUT2	Output 2
18	OUT1	Output 1
19	OUT0	Output 0
20	M1	Mode Pin 1
21	M0	Mode Pin 0
22	CLK	Main Clock
23	RST_N	Reset
24	VDDIO	IO Power Supply
25	I2C_SCL	I2C / SPI / SPIM Clock
26	I2C_SDA	I2C Data / SPI Slave Select
27	I2C_A0	I2C Slave Address Bit 0 / SPI_MOSI / SPIM_MOSI
28	I2C_A1	I2C Slave Address Bit 1 / SPI_MISO / SPIM_MISO
29	SPIM_SS_N	SPI Master Slave Select
30	PDM_CLK	PDM Clock
31	PDM_DATA	PDM Data
32	VDDIO	IO Power Supply

Make Intelligence Smarter